6.17.8 Trap Detect Logic

The purpose of the trap detect logic in Figure 6-34 is to generate an INT RQST if an IOT, HLT, LAS, or OSR instruction is executed by a user program while the computer is in the User Mode. NAND gate E11 is enabled by KMTS2 USER MODE H when S2-1 on is set to off. TP2 H is used to enable the input to INTERRUPT flip-flop so that an INT RQST will not be made until the completion of the current memory cycle. Any interrupt returns the computer to Executive Mode and the timesharing system monitor must determine what to do about the interrupt.

The SINT instruction asserts SKIP L if the USER INTERRUPT flip-flop is set. This instruction is used for flag checking routines.

The CINT instruction clears the USER INTERRUPT flip-flop.

6.17.9 Interrupt Inhibit Logic

The Interrupt Inhibit flip-flop in Figure 6-35 is set by KMTS2+1 INT INH H, which is asserted (high) if a CIF, CUF, SUF, RMF, or RTF instruction is executed by the program and S2-1 is off (see Figure 6-33). S2-1 is set to off to enable the Timeshare Mode. When the INTERRUPT INHIBIT flip-flop sets, INT IN PROG L is asserted (low) and the interrupt system is turned off. Interrupt Inhibit is cleared when a JMP or JMS instruction is executed at the end of an interrupt service routine. Also at this time the IF and DF registers are restored from the Save Field registers or loaded with a new field.

6.18 POWER FAIL/AUTO RESTART AND BOOTSTRAP LOADER

The Power Fail/Auto Restart and Bootstrap options are discussed in the following paragraphs.

6.18.1 Power Fail/Auto Restart Block Diagram Description

The power supply monitors the ac line voltage and detects when the ac line voltage has fallen below a certain level, (95 V ±3% for 117 Vac operation), and generates a logic signal AC LOW. This signal causes logic in the Power Fail/Auto Restart portion of the KM8-A extended option board to interrupt the program, which takes the necessary action as the ac power is going away (Figure 6-35). In MOS memory systems, the automatic switch-over to a battery supply that allows the system to continue operation for an additional 45 seconds minimum, will occur. If power is restored during this time, the system will automatically switch back to the regular power supply. In core memory systems, the program should store all active registers (AC, MQ, etc.) and stop the system when a low ac voltage is detected. The computer will restart and the program can restore the active registers when ac power goes above 105 Vac (117 Vac operation.)

Features

Restart Address:	One of four restart addresses may be selected, one at a time (4200, 2000, 0200, or 0000).
Auto Restart:	If Auto Restart is enabled, the PDP-8/A starts automatically when power is applied. This allows the user to apply power remotely and start the system without going to the PDP-8/A. (Auto-Start on the CPU must be disabled.)

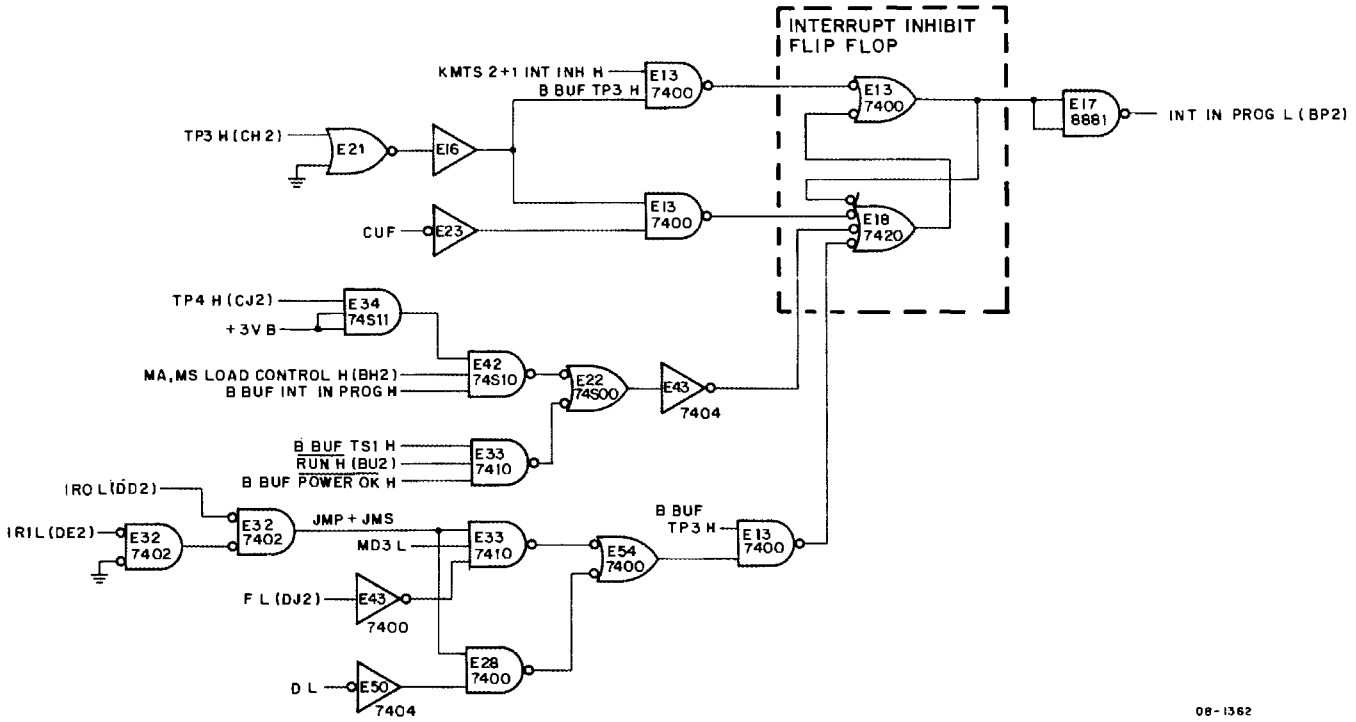


Figure 6-35 Interrupt Inhibit Logic

6.18.2 Power Fail/Auto Restart Programming (Figure 6-36)

The IOT instructions used with the Power Fail/Auto Restart option are as follows:

Mnemonic	Octal Code	Function
SPL	6102	Skip if the AC LOW flag is set or AC LOW signal is low. After detecting an AC LOW condition, flag should be cleared by a CAL instruction. Then test using the SPL instruction until ac goes above 105 V. Then test by an SPL instruction to skip on the level AC LOW being low. The INT RQST line will not be asserted after the flag has been cleared by CAL.
CAL	6103	Clear the AC LOW interrupt.
SBE	6101	Skip if the BATTERY EMPTY flag is set.

The device code for this option is fixed as 10.

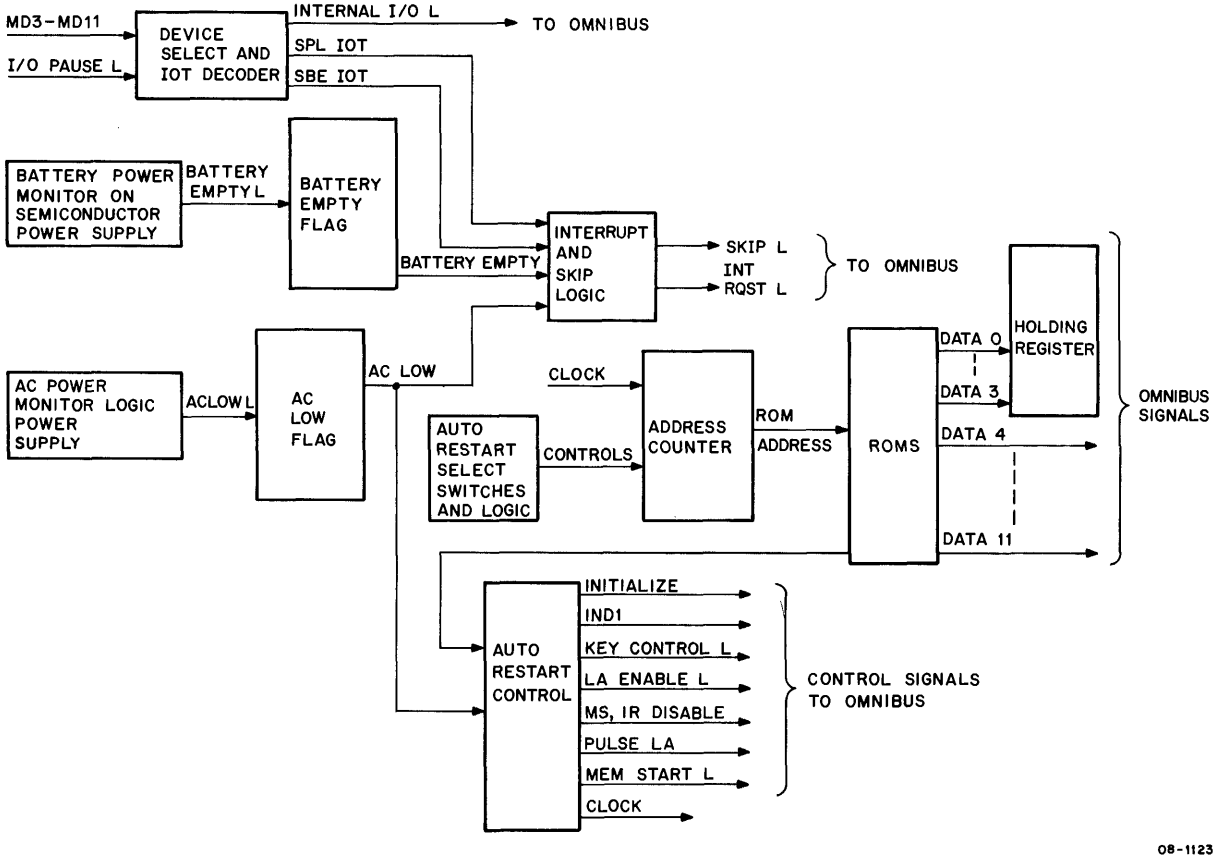


Figure 6-36 Power Fail and Auto Restart Block Diagram

6.18.3 Bootstrap Loader Block Diagram Description

The Bootstrap Loader (Figure 6-37) on the M8317 module provides the logic to deposit one of several programs that is contained in two ROMs on the M8317 module into read/write memory. These programs provide the necessary instructions to load programs from paper tape, disk, magnetic tape, etc., and to start the program at the specified location.

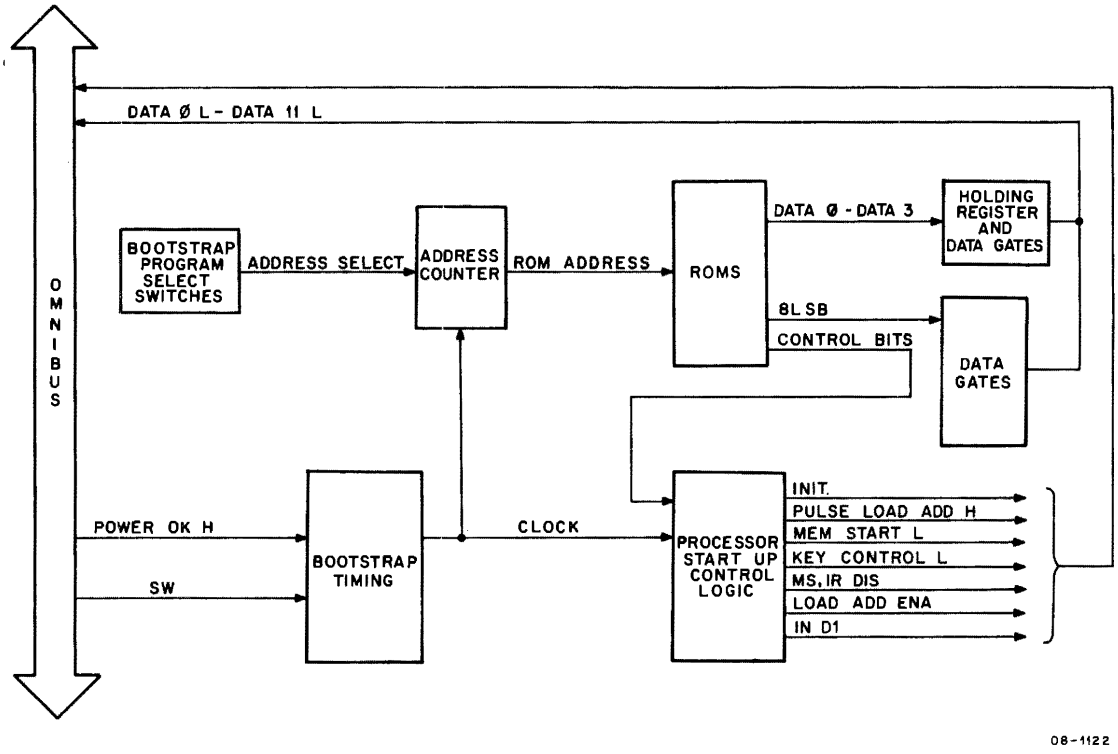


Figure 6-37 Bootstrap Loader Block Diagram

The Bootstrap Loader may be activated by pressing the BOOT switch on the Limited Function Panel or the optional Programmer's Console or from the transition of AC LOW from low to high. The computer must be halted for AC LOW to activate the bootstrap. Two switches on the M8317 module select the appropriate signal to activate the bootstrap.

The bootstrap can be started when the computer is turned on. This feature is enabled by a switch on the M8317 and allows the computer to be started remotely when the PDP-8/A is used as a peripheral.

6.19 BOOTSTRAP ROM ORGANIZATION AND PROGRAMMING

For those users who wish to write their own program into the bootstrap ROMs, the following procedures should be used.

6.19.1 ROM Organization

The two ROMs are connected as follows: the address lines are connected in parallel, i.e., two corresponding address lines of each ROM are connected together, and the outputs are arranged in serial fashion forming an 8-bit word, 4 outputs from each ROM. Because 12 bits are required for data/address information, two sequential addresses must be accessed from the ROMs to form a 16-bit word. Where the first 8 bits are temporarily stored in a register, then the next 8 bits are accessed from the ROMs. At this point, the control then decides what to do with 12 of the 16 bits. There are four possible actions that can take place at this time:

1. Load Address
2. Load Extended Address
3. Deposit
4. Start

The remaining 4 bits of the 16 actually tell the control which of the four actions are to take place. The 16-bit word should look like the word in Figure 6-38.

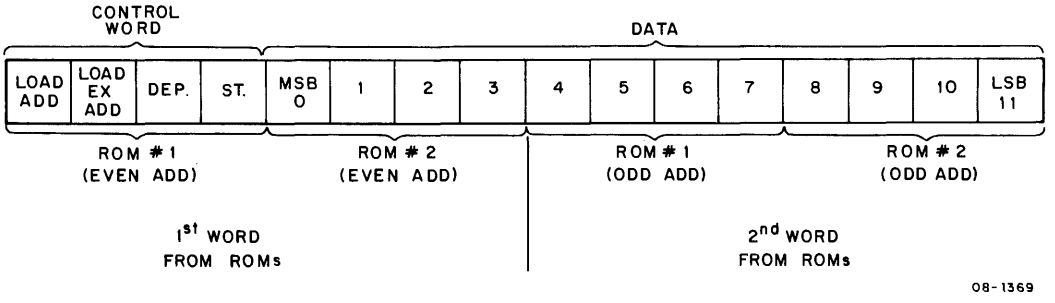


Figure 6-38 16 Bit Word ROM Format

The use of ROMs that have 256 addressable locations allows up to 128 words of ROM storage. These 128 locations may be used for bootstrap and/or auto-restart programs. Any auto-restart or bootstrap program may be located anywhere in the ROMs as long as the program starts in an even address in the ROM. If it is required that both bootstrap and auto-restart programs be accessible at the same time, activated by different signals, then of course the auto-restart program(s) must be located in addresses 0 through 15 in the ROMs. This is due to the addressing limits of the auto-restart select switches.

6.19.2 Auto-Restart/Bootstrap Sequence

The following events should take place when an auto-restart is initiated:

1. Load a 12 bit address
2. Load the extended address and start.

The following events should take place when the bootstrap is initiated:

1. Load a 12 bit initial address.
2. Load the Extended Address.
3. Deposit 12-bit data words, repeating as required by length of program, to be deposited.
4. Load a 12-bit starting address and start.

The decision to perform a bootstrap or an auto-restart is directed by a set of switches on the module. The bootstrap may be activated by the transition of the signal AC LOW from a logic low to a logical high or by a similar transition of the SW line on the Omnibus.

Auto-restart is only activated by AC LOW.

6.19.3 ROM Programming Examples

An auto-restart example is shown in Figure 6-39.

1. Load address 0200
2. Load field 0, start

Starting at ROM address 004.

	ROM NO. 1				ROM NO. 2				
Bit / Add	4	3	2	1	4	3	2	1	
4	1	0	0	0	0	0	0	0	Load Address 0200
5	1	0	0	0	0	0	0	0	
6	0	1	0	1	0	0	0	0	Load Ext. Add 0 and Start
7	0	0	0	0	0	0	0	0	

NOTE: Logic one (1) = + 3V

Figure 6-39 Auto Restart Example

6.19.4 Bootstrap Example (Figure 6-40)

1. Load address 0023
2. Load field 7
3. Deposit 2000
4. Deposit 6745
5. Deposit 0023
6. Deposit 7650
7. Deposit 5024
8. Deposit 6733
9. Deposit 5031
10. Load address 0024 and start

Starting at ROM address 124.

6.19.5 Obtaining Blank ROMs

Unprogrammed ROMs should be purchased by the user from Digital Equipment Corporation. The part number for an unprogrammed 256 X 4 ROM is 23-000A8.

	ROM NO. 1				ROM NO. 2				
Bit Add	4	3	2	1	4	3	2	1	
124	1	0	0	0	0	0	0	0	} Load Add 0023
125	0	0	0	1	0	0	1	1	
126	0	1	0	0	0	0	0	0	} Load Ext Add 7
127	0	0	1	1	1	0	0	0	
130	0	0	1	0	0	1	0	0	} Dep 2000
131	0	0	0	0	0	0	0	0	
132	0	0	1	0	1	1	0	1	} Dep 6745
133	1	1	1	0	0	1	0	1	
134	0	0	1	0	0	0	0	0	} Dep 0023
135	0	0	0	1	0	0	1	1	
136	0	0	1	0	1	1	1	1	} Dep 7650
137	1	0	1	0	1	0	0	0	
140	0	0	1	0	1	0	1	0	} Dep 5024
141	0	0	0	1	0	1	0	0	
142	0	0	1	0	1	1	0	1	} Dep 6733
143	1	1	0	1	1	0	1	1	
144	0	0	1	0	1	0	1	0	} Dep 5031
145	0	0	0	1	1	0	0	1	
146	1	0	0	1	0	0	0	0	} Load Add 24 & Start
147	0	0	0	1	0	1	0	0	

Figure 6-40 Bootstrap Example

6.20 ROM PROGRAM LISTING

All M8317 modules are shipped with the programs in either Table 6-6 or Table 6-7 stored in ROM No. 1 and ROM No. 2. The ROM patterns for these ROMs are listed in the KM8-A print set in Appendix H.

6.21 POWER FAIL/AUTO RESTART AND BOOTSTRAP OPERATION AND TIMING

6.21.1 Power Fail Operation

The power fail portion of the M8317 module initiates a controlled shutdown sequence when a power failure occurs. Circuits in the power supply monitor the ac voltage (Paragraph 7.2) and generate AC LOW L when the voltage falls below a predetermined level. In the 8A core memory systems, AC LOW L causes an INT RQST and the program must take the necessary action to store all active registers while the dc supply is adequate to maintain system operation. INT RQST is also asserted in these machines by ac power going low even though they switch to battery power. In the PDP-8/A Semiconductor memory system, operation is switched to battery power automatically when ac power fails. If ac power is not restored a fully loaded system will continue to run for up to 45 seconds. If ac power is restored, system operation is switched back to the regular power supply when they are in regulation. If power is not restored after a period of approximately 45 seconds, the BATTERY EMPTY signal is asserted and causes an INT RQST. At this time the program has 1 ms to do whatever is necessary to shut down the system before battery power is removed. When power is removed completely, the content of the MS8-A RAM is lost and programs in this memory must be reloaded.

Table 6-6
ROM No. 1 and ROM No. 2 Listings
(for ROMs Labeled 87A2 and 88A2)

ROM ADDRESS	MEMORY ADDRESS	CONTENTS (ROM and/or MEMORY)	COMMENTS
0	0000	0000	AUTO/RESTART
1			LOAD ADDRESS 0000
2	0000	0000	AUTO/RESTART
3			LOAD FIELD 0/START
4	0200	0200	AUTO/RESTART
5			LOAD ADDRESS 0200
6	0000	0000	AUTO-RESTART
7			LOAD FIELD 0/START
10	2000	2000	AUTO-RESTART
11			LOAD ADDRESS 2000
12	0000	0000	AUTO-RESTART
13			LOAD FIELD 0/START
14	4200	4200	AUTO-RESTART
15			LOAD ADDRESS 4200
16	0000	0000	AUTO-RESTART
17			LOAD FIELD 0/START
20	7737	7737	HIGH-LOW PAPERTAPE
21			LOAD ADDRESS 7737
22	0000	0000	LOAD FIELD 0
23			
24	7737	6014	DEPOSIT 6014
25			
26	7740	3376	DEPOSIT 3376
27			
30	7741	7326	DEPOSIT 7326
31			
32	7742	1337	DEPOSIT 1337
33			
34	7743	2376	DEPOSIT 2376
35			
36	7744	5341	DEPOSIT 5341
37			
40	7745	6011	DEPOSIT 6011
41			
42	7746	5356	DEPOSIT 5356
43			
44	7747	3361	DEPOSIT 3361
45			
46	7750	1361	DEPOSIT 1361
47			
50	7751	3371	DEPOSIT 3371
51			
52	7752	1345	DEPOSIT 1345
53			
54	7753	3357	DEPOSIT 3357
55			

Table 6-6 (Cont)
ROM No. 1 and ROM No. 2 Listings
(for ROMs Labeled 87A2 and 88A2)

ROM ADDRESS	MEMORY ADDRESS	CONTENTS (ROM and/or MEMORY)	COMMENTS
56	7754	1345	DEPOSIT 1345
57			
60	7755	3367	DEPOSIT 3367
61			
62	7756	6032	DEPOSIT 6032
63			
64	7757	6031	DEPOSIT 6031
65			
66	7760	5357	DEPOSIT 5357
67			
70	7761	6036	DEPOSIT 6036
71			
72	7762	7106	DEPOSIT 7106
73			
74	7763	7006	DEPOSIT 7006
75			
76	7764	7510	DEPOSIT 7510
77			
100	7765	5374	DEPOSIT 5374
101			
102	7766	7006	DEPOSIT 7006
103			
104	7767	6031	DEPOSIT 6031
105			
106	7770	5367	DEPOSIT 5367
107			
110	7771	6034	DEPOSIT 6034
111			
112	7772	7420	DEPOSIT 7420
113			
114	7773	3776	DEPOSIT 3776
115			
116	7774	3376	DEPOSIT 3376
117			
120	7775	5356	DEPOSIT 5356
121			
122	7737	7737	LOAD ADDRESS 7737/
123			START
124	0023	0023	RK8/E
125			LOAD ADDRESS 23
126	0000	0000	LOAD FIELD 0
127			
130	0023	2200	DEPOSIT 2200
131			
132	0024	6745	DEPOSIT 6745
133			

Table 6-6 (Cont)
ROM No. 1 and ROM No. 2 Listings
(for ROMs Labeled 87A2 and 88A2)

ROM ADDRESS	MEMORY ADDRESS	CONTENTS (ROM and/or MEMORY)	COMMENTS
134	0025	0023	DEPOSIT 0023
135			
136	0026	7640	DEPOSIT 7640
137			
140	0027	5024	DEPOSIT 5024
141			
142	0030	6743	DEPOSIT 6743
143			
144	0031	5031	DEPOSIT 5031
145			
146	0024	0024	LOAD ADDRESS 24/
147			START
150	7613	7613	TC08
151			LOAD ADDRESS 7613
152	0000	0000	LOAD FLD 0
153			
154	7613	6774	DEPOSIT 6774
155			
156	7614	1222	DEPOSIT 1222
157			
160	7615	6766	DEPOSIT 6766
161			
162	7616	6771	DEPOSIT 6771
163			
164	7617	5216	DEPOSIT 5216
165			
166	7620	1223	DEPOSIT 1223
167			
170	7621	5215	DEPOSIT 5215
171			
172	7622	0600	DEPOSIT 0600
173			
174	7623	0220	DEPOSIT 0220
175			
176	7754	7754	LOAD ADDRESS
177			7754
200	7754	7577	DEPOSIT 7577
201			
202	7755	7577	DEPOSIT 7577
203			
204	7613	7613	LOAD ADDRESS 7613/
205			START
206	7750	7750	RF08/DF32D
207			LOAD ADDRESS 7750
210	0000	0000	LOAD FIELD 0
211			

Table 6-6 (Cont)
ROM No. 1 and ROM No. 2 Listings
(for ROMs Labeled 87A2 and 88A2)

ROM ADDRESS	MEMORY ADDRESS	CONTENTS (ROM and/or MEMORY)	COMMENTS
212	7750	7600	DEPOSIT 7600
213			
214	7751	6603	DEPOSIT 6603
215			
216	7752	6622	DEPOSIT 6622
217			
220	7753	5352	DEPOSIT 5352
221			
222	7754	5752	DEPOSIT 5752
223			
224	7750	7750	LOAD ADDRESS 7750/
225			START
226	4000	4000	TA8/E
227			LOAD ADDRESS 4000
230	0000	0000	LOAD FIELD 0
231			
232	4000	1237	DEPOSIT 1237
233			
234	4001	1206	DEPOSIT 1206
235			
236	4002	6704	DEPOSIT 6704
237			
240	4003	6706	DEPOSIT 6706
241			
242	4004	6703	DEPOSIT 6703
243			
244	4005	5204	DEPOSIT 5204
245			
246	4006	7264	DEPOSIT 7264
247			
250	4007	6702	DEPOSIT 6702
251			
252	4010	7610	DEPOSIT 7610
253			
254	4011	3211	DEPOSIT 3211
255			
256	4012	3636	DEPOSIT 3636
257			
260	4013	1205	DEPOSIT 1205
261			
262	4014	6704	DEPOSIT 6704
263			
264	4015	6706	DEPOSIT 6706
265			
266	4016	6701	DEPOSIT 6701
267			

Table 6-6 (Cont)
ROM No. 1 and ROM No. 2 Listings
(for ROMs Labeled 87A2 and 88A2)

ROM ADDRESS	MEMORY ADDRESS	CONTENTS (ROM and/or MEMORY)	COMMENTS
270	4017	5216	DEPOSIT 5216
271			
272	4020	7002	DEPOSIT 7002
273			
274	4021	7430	DEPOSIT 7430
275			
276	4022	1636	DEPOSIT 1636
277			
300	4023	7022	DEPOSIT 7022
301			
302	4024	3636	DEPOSIT 3636
303			
304	4025	7420	DEPOSIT 7420
305			
306	4026	2236	DEPOSIT 2236
307			
310	4027	2235	DEPOSIT 2235
311			
312	4030	5215	DEPOSIT 5215
313			
314	4031	7346	DEPOSIT 7346
315			
316	4032	7002	DEPOSIT 7002
317			
320	4033	3235	DEPOSIT 3235
321			
322	4034	5201	DEPOSIT 5201
323			
324	4035	7737	DEPOSIT 7737
325			
326	4036	3557	DEPOSIT 3557
327			
330	4037	7730	DEPOSIT 7730
331			
332	4000	4000	LOAD ADDRESS 4000/
333			START
334 to 377	Spare Locations (36(10) ROM Address) (18(10) Words)		

Table 6-7
ROM No. 1 and ROM No. 2 Listings
(for ROMs Labeled 158A2 and 159A2)

ROM ADDRESS	MEMORY ADDRESS	CONTENTS (ROM and/or MEMORY)	COMMENTS
0	0000	0000	AUTO/RESTART
1			LOAD ADDRESS 0000
2	0000	0000	AUTO/RESTART
3			LOAD FIELD 0/START
4	0200	0200	AUTO/RESTART
5			LOAD ADDRESS 0200
6	0000	0000	AUTO-RESTART
7			LOAD FIELD 0/START
10	2000	2000	AUTO-RESTART
11			LOAD ADDRESS 2000
12	0000	0000	AUTO-RESTART
13			LOAD FIELD 0/START
14	4200	4200	AUTO-RESTART
15			LOAD ADDRESS 4200
16	0000	0000	AUTO-RESTART
17			LOAD FIELD 0/START
20	7737	7737	HIGH-LOW PAPERTAPE
21			LOAD ADDRESS 7737
22	0000	0000	LOAD FIELD 0
23			
24	7737	6014	DEPOSIT 6014
25			
26	7740	3376	DEPOSIT 3376
27			
30	7741	7326	DEPOSIT 7326
31			
32	7742	1337	DEPOSIT 1337
33			
34	7743	2376	DEPOSIT 2376
35			
36	7744	5341	DEPOSIT 5341
37			
40	7745	6011	DEPOSIT 6011
41			
42	7746	5356	DEPOSIT 5356
43			
44	7747	3361	DEPOSIT 3361
45			
46	7750	1361	DEPOSIT 1361
47			
50	7751	3371	DEPOSIT 3371
51			
52	7752	1345	DEPOSIT 1345
53			
54	7753	3357	DEPOSIT 3357
55			

Table 6-7 (Cont)
ROM No. 1 and ROM No. 2 Listings
(for ROMs Labeled 158A2 and 159A2)

ROM ADDRESS	MEMORY ADDRESS	CONTENTS (ROM and/or MEMORY)	COMMENTS
56	7754	1345	DEPOSIT 1345
57			
60	7755	3367	DEPOSIT 3367
61			
62	7756	6032	DEPOSIT 6032
63			
64	7757	6031	DEPOSIT 6031
65			
66	7760	5357	DEPOSIT 5357
67			
70	7761	6036	DEPOSIT 6036
71			
72	7762	7106	DEPOSIT 7106
73			
74	7763	7006	DEPOSIT 7006
75			
76	7764	7510	DEPOSIT 7510
77			
100	7765	5374	DEPOSIT 5374
101			
102	7766	7006	DEPOSIT 7006
103			
104	7767	6031	DEPOSIT 6031
105			
106	7770	5367	DEPOSIT 5367
107			
110	7771	6034	DEPOSIT 6034
111			
112	7772	7420	DEPOSIT 7420
113			
114	7773	3776	DEPOSIT 3776
115			
116	7774	3376	DEPOSIT 3376
117			
120	7775	5356	DEPOSIT 5356
121			
122	7737	7737	LOAD ADDRESS 7737/
123			START
124	0023	0023	RK8/E
125			LOAD ADDRESS 23
126	0000	0000	LOAD FIELD 0
127			
130	0023	2200	DEPOSIT 2200
131			
132	0024	6745	DEPOSIT 6745
133			

Table 6-7 (Cont)
ROM No. 1 and ROM No. 2 Listings
(for ROMs Labeled 158A2 and 159A2)

ROM ADDRESS	MEMORY ADDRESS	CONTENTS (ROM and/or MEMORY)	COMMENTS
134	0025	0023	DEPOSIT 0023
135			
136	0026	7640	DEPOSIT 7640
137			
140	0027	5024	DEPOSIT 5024
141			
142	0030	6743	DEPOSIT 6743
143			
144	0031	5031	DEPOSIT 5031
145			
146	0024	0024	LOAD ADDRESS 24/
147			START
150	0024	0024	RX8E
151			LOAD ADDRESS 0024
152	0000	0000	LOAD FIELD 0
153			
154	0024	7126	DEPOSIT 7126
155			
156	0025	1060	DEPOSIT 1060
157			
160	0026	6751	DEPOSIT 6751
161			
162	0027	7201	DEPOSIT 7201
163			
164	0030	4053	DEPOSIT 4053
165			
166	0031	4053	DEPOSIT 4053
167			
170	0032	7104	DEPOSIT 7104
171			
172	0033	6755	DEPOSIT 6755
173			
174	0034	5054	DEPOSIT 5054
175			
176	0035	6754	DEPOSIT 6754
177			
200	0036	7450	DEPOSIT 7450
201			
202	0037	7610	DEPOSIT 7610
203			
204	0040	5046	DEPOSIT 5046
205			
206	0041	1060	DEPOSIT 1060
207			
210	0042	7041	DEPOSIT 7041
211			

Table 6-7 (Cont)
ROM No. 1 and ROM No. 2 Listings
(for ROMs Labeled 158A2 and 159A2)

ROM ADDRESS	MEMORY ADDRESS	CONTENTS (ROM and/or MEMORY)	COMMENTS
212	0043	1061	DEPOSIT 1061
213			
214	0044	3060	DEPOSIT 3060
215			
216	0045	5024	DEPOSIT 5024
217			
220	0046	6751	DEPOSIT 6751
221			
222	0047	4053	DEPOSIT 4053
223			
224	0050	3002	DEPOSIT 3002
225			
226	0051	2050	DEPOSIT 2050
227			
230	0052	5047	DEPOSIT 5047
231			
232	0053	0000	DEPOSIT 0000
233			
234	0054	6753	DEPOSIT 6753
235			
236	0055	5033	DEPOSIT 5033
237			
240	0056	6752	DEPOSIT 6752
241			
242	0057	5453	DEPOSIT 5453
243			
244	0060	7024	DEPOSIT 7024
245			
246	0061	6030	DEPOSIT 6030
247			
250	0033	0033	LOAD ADDRESS 0033/
251			START
252	7750	7750	RF08/DF32D
253			LOAD ADDRESS 7750
254	0000	0000	LOAD FIELD 0
255			
256	7750	7600	DEPOSIT 7600
257			
260	7751	6603	DEPOSIT 6603
261			
262	7752	6622	DEPOSIT 6622
263			
264	7753	5352	DEPOSIT 5352
265			
266	7754	5752	DEPOSIT 5752
267			

Table 6-7 (Cont)
ROM No. 1 and ROM No. 2 Listings
(for ROMs Labeled 158A2 and 159A2)

ROM ADDRESS	MEMORY ADDRESS	CONTENTS (ROM and/or MEMORY)	COMMENTS
270	7750	7750	LOAD ADDRESS 7750/
271			START
272	4000	4000	TA8/E
273			LOAD ADDRESS 4000
274	0000	0000	LOAD FIELD 0
275			
276	4000	1237	DEPOSIT 1237
277			
300	4001	1206	DEPOSIT 1206
301			
302	4002	6704	DEPOSIT 6704
303			
304	4003	6706	DEPOSIT 6706
305			
306	4004	6703	DEPOSIT 6703
307			
310	4005	5204	DEPOSIT 5204
311			
312	4006	7264	DEPOSIT 7264
313			
314	4007	6702	DEPOSIT 6702
315			
316	4010	7610	DEPOSIT 7610
317			
320	4011	3211	DEPOSIT 3211
321			
322	4012	3636	DEPOSIT 3636
323			
324	4013	1205	DEPOSIT 1205
325			
326	4014	6704	DEPOSIT 6704
327			
330	4015	6706	DEPOSIT 6706
331			
332	4016	6701	DEPOSIT 6701
333			
334	4017	5216	DEPOSIT 5216
335			
336	4020	7002	DEPOSIT 7002
337			
340	4021	7430	DEPOSIT 7430
341			
342	4022	1636	DEPOSIT 1636
343			
344	4023	7022	DEPOSIT 7022
345			

Table 6-7 (Cont)
ROM No. 1 and ROM No. 2 Listings
(for ROMs Labeled 158A2 and 159A2)

ROM ADDRESS	MEMORY ADDRESS	CONTENTS (ROM and/or MEMORY)	COMMENTS
346	4024	3636	DEPOSIT 3636
347			
350	4025	7420	DEPOSIT 7420
351			
352	4026	2236	DEPOSIT 2236
353			
354	4027	2235	DEPOSIT 2235
355			
356	4030	5215	DEPOSIT 5215
357			
360	4031	7346	DEPOSIT 7346
361			
362	4032	7002	DEPOSIT 7002
363			
364	4033	3235	DEPOSIT 3235
365			
366	4034	5201	DEPOSIT 5201
367			
370	4035	7737	DEPOSIT 7737
371			
372	4036	3557	DEPOSIT 3557
373			
374	4037	7730	DEPOSIT 7730
375			
376	4000	4000	LOAD ADDRESS 4000/ START
377			

6.21.2 Auto-Restart Operation and Timing

The auto-restart portion of the M8317 module restarts the PDP-8/A after a power failure or when power is turned on locally or remotely. The program may be started at address 4200, 2000, 0200, or 0000. The address is switch selectable on the M8317 module.

The computer must start by executing the instruction stored in the starting location.

The CPMA register and the IF and DF registers in the memory extension portion of the M8317 module must be loaded with the starting address before CPU timing is allowed to start. Before start-up, all devices must be initialized and the Major State register must be manipulated so that it starts out in the Fetch major state. The auto-restart logic accomplishes this by asserting the Omnibus signals and performing transfers that normally occur from the Programmer's Console.

At the Programmer's Console, the start-up procedure is as follows:

1. Enter the Instruction Field and Data Field and press LXA (load DF and IF registers).
2. Enter starting address and press LA .
3. Press INIT and then RUN (Initialize and start from FETCH).

These operations are performed by the auto-restart portion of the KM8-AA.

The timing for this operation is shown in Figure 6-41. The detailed logic description of this operation is given in Paragraph 6.22.

The starting addresses (0000, 0200, 2000 and 4200) are stored in a 256 X 8 ROM along with the necessary control bits. The first ROM address to be accessed when the auto-restart operation begins is determined by switches on the M8317 module which preset the ROM address counter to this first address. The address counter is then incremented to read four ROM memory locations, which supply the field, the starting address and the necessary control signals required to load the field and starting address, initialize the processor, and start the program. Four of the 256 ROM locations are used for each of the starting addresses, a total of 16 addresses for the auto-restart operation. Except for the last 43 locations, the remainder of the ROM chip is used for bootstrap operation. (Refer to Table 6-6 and Figure 6-40).

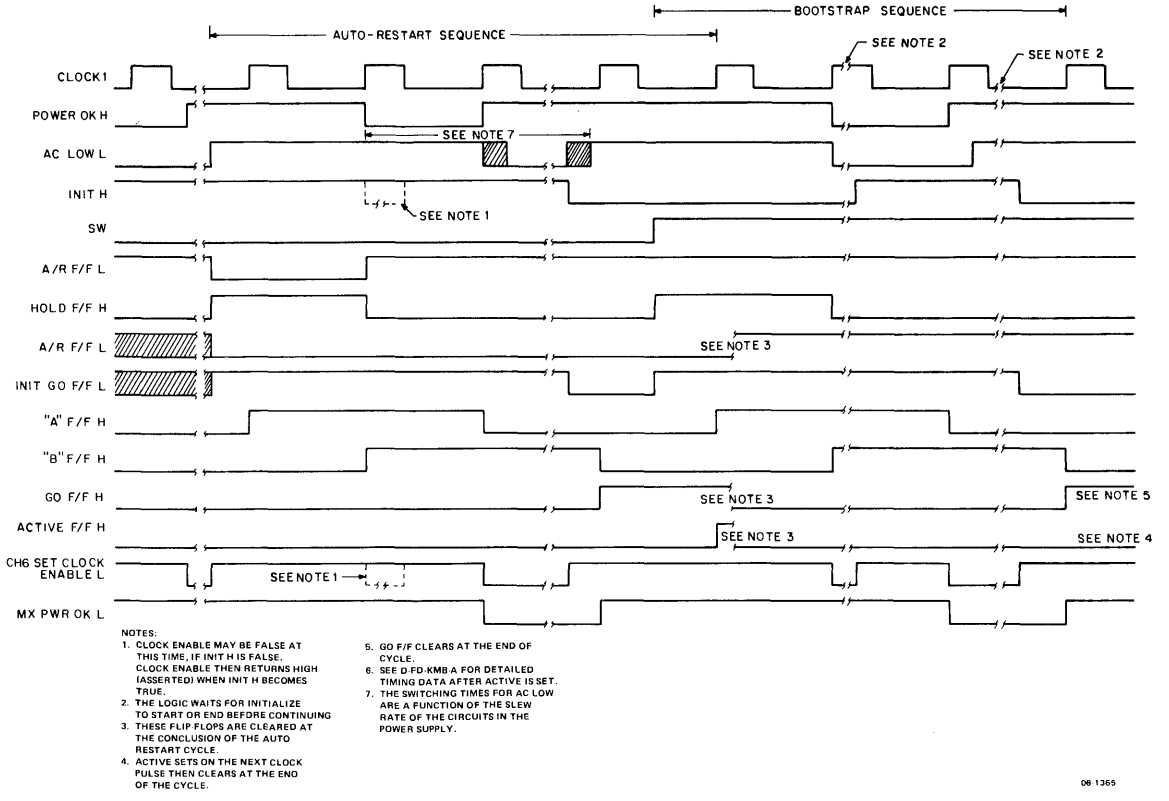


Figure 6-41 Auto Restart and Bootstrap Timing

6.21.3 Bootstrap Operation and Timing

The bootstrap operation portion of the M8317 logic is used to load short programs into memory which are used to load programs from system devices and to start the program at the specified location. A bootstrap operation is initiated by pressing BOOT on the Programmer's Console twice or by raising and lowering the BOOT switch on the Limited Function Panel.

When the Bootstrap operation is initiated the following occurs:

1. The CPU is initialized.
2. Load extended address and starting address to define the first address in which to deposit instructions.
3. Deposit instructions in sequential locations.
4. Load the starting address of the program just deposited.
5. Start the program.

In this operation the content specified locations in the 256 X 8 ROM is used to furnish the field, starting address, control signals, and programmed instructions required to transfer a program from a system device (Table 6-6). The specified location in ROM from which this information is obtained is determined by switches on the M8317 module.

The timing required for this operation is shown in Figures 6-41 and 6-42. The detailed logic description of this operation is given in Paragraph 6.22.

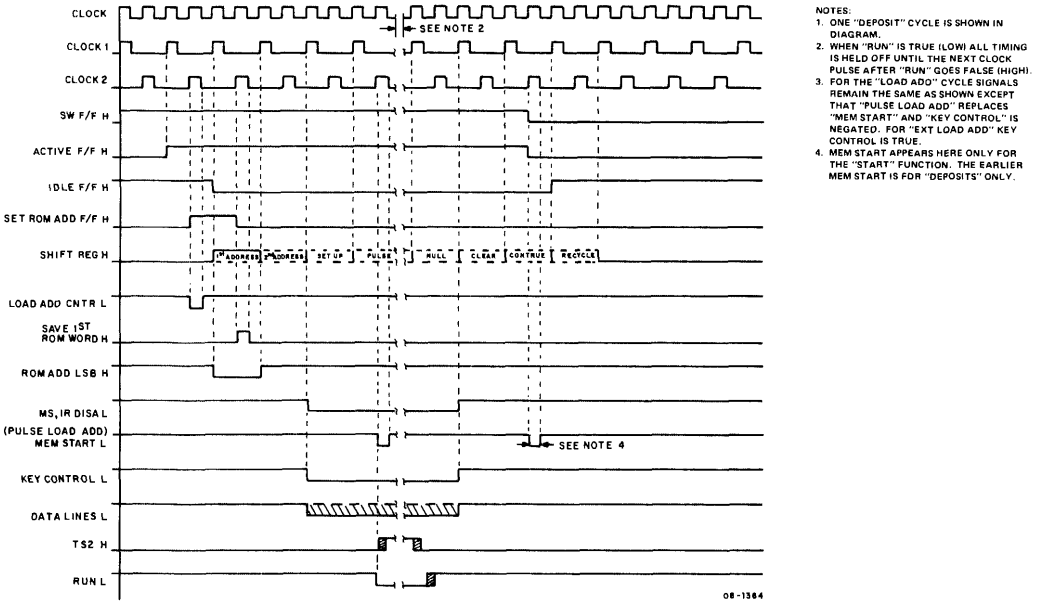


Figure 6-42 Bootstrap Timing

6.22 POWER FAIL/AUTO-RESTART AND BOOTSTRAP OPERATION DETAILED LOGIC DESCRIPTION

Some of the functional groups of logic on the M8317 are shared by the power fail/auto-restart and the bootstrap option. During this discussion it will be pointed out that when a functional group of logic applies to only one of the operations, or if it applies to more than one operation and its use. The block diagrams in Figures 6-36 and 6-37 should be used to determine which groups of logic are used by the individual operations and the interrelationship between the groups of logic as well as the signal flow.

6.22.1 Power Fail/Auto-Restart Device Select and Operation Decoder

The Power Fail/Auto-Restart device select and operation decoder logic is shown in Figure 6-43.

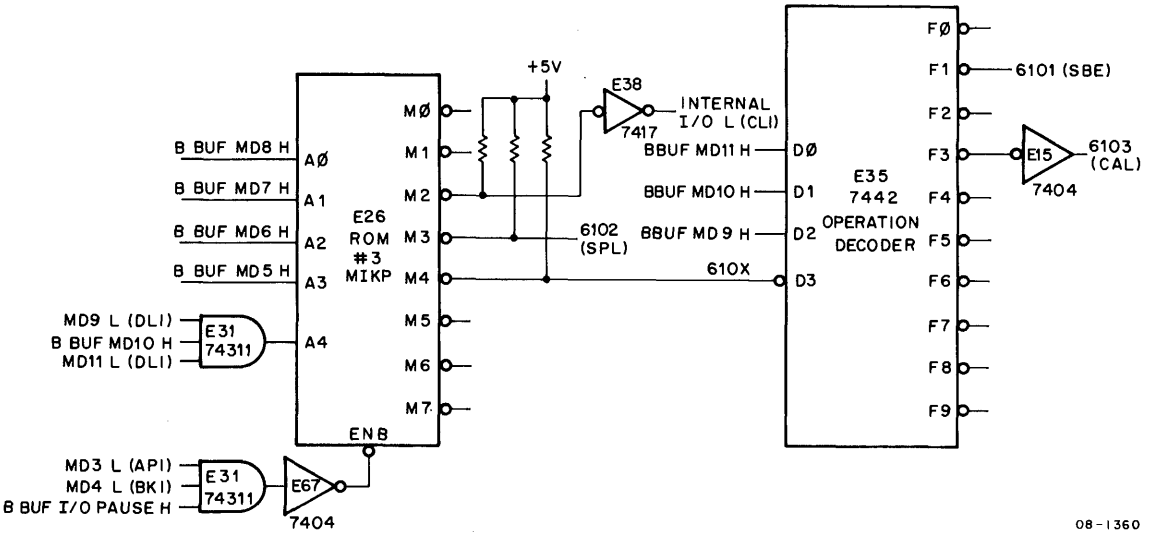


Figure 6-43 Power Fail Auto Restart Device Select and Operation Decoder

ROM No. 3, the device select decoder, is enabled by MD3 L, MD4 L and BBUF I/O PAUSE H when a 61XX instruction is executed by the program. When the ROM is enabled, it is addressed by BBUF MD5 H-BBUF MD8 H and the AND of MD9 L, BBUF MD10 H, and MD11 L. When a 610X instruction is executed by the program, the ROM address selected supplies an output which asserts INTERNAL I/O L and the 610X device select signal. INTERNAL I/O L is asserted to tell the KA8-E Positive I/O that the instruction is not to be decoded by the KA8-E. The 610X signal enables the operation decoder to decode the 6101 and 6103 instructions. When the program executes a 6102 (SPL) instruction the output of AND gate E31 adds an additional bit to the ROM address to select the location with an output which asserts INTERNAL I/O L and the 6102 signal line.

This causes the power fail/auto-restart option to execute the 6102 instruction.

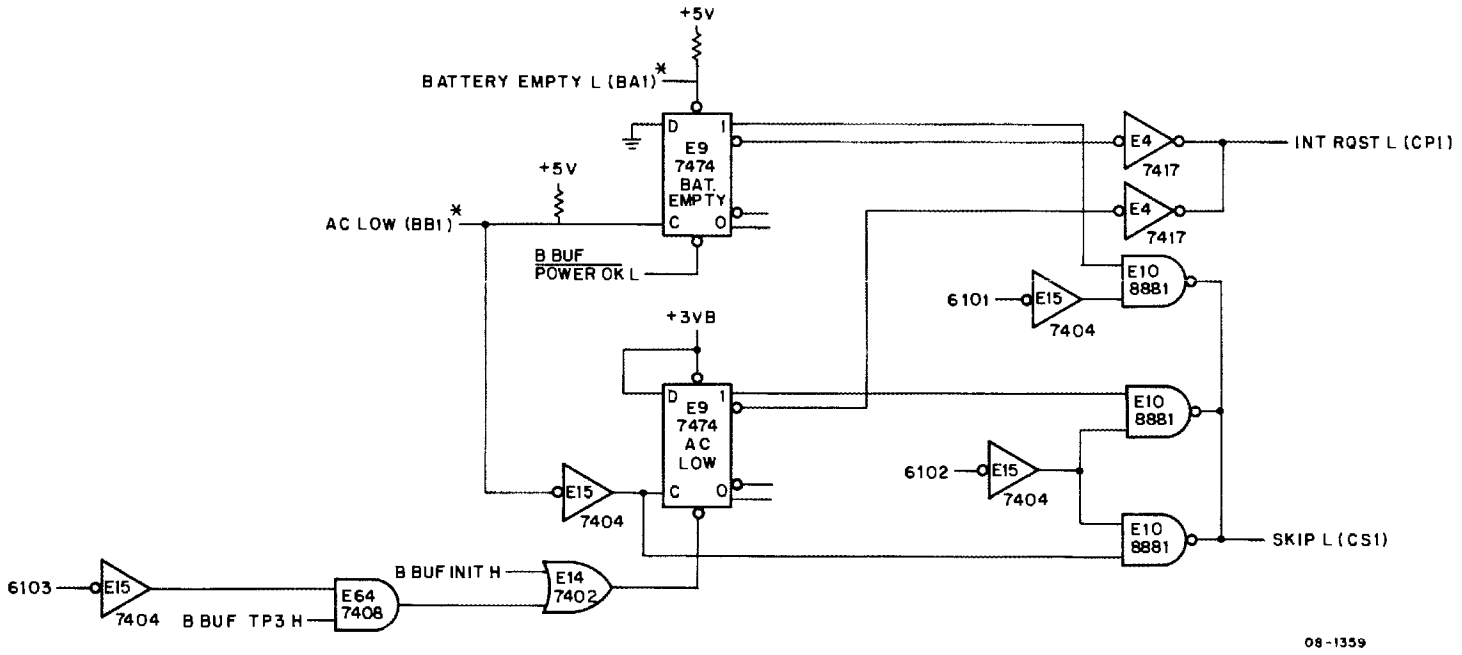
The operation decoder is enabled by the 610X signal when a 610X instruction is decoded by the program. The operation decoder is a 7442 IC. The 7442 IC is a BCD to decimal decoder which decodes BBUF MD9-BBUF MD10 and asserts the necessary signals to execute the 6107 and 6103 instructions.

6.22.2 Power Fail Interrupt and Skip Logic

The power fail interrupt and skip logic is shown in Figure 6-44. There are two flags associated with SKIP L and INT RQST L – 1. The AC LOW flag, which is set by AC LOW L from the power supply when the ac voltage falls below a specified level, and 2. the BATTERY EMPTY flag, which sets when BATTERY EMPTY L is asserted by the power supply logic (applicable only to PDP-8/A Semiconductor computers). BATTERY EMPTY L is asserted prior to depletion of the battery so that the battery will never completely discharge. A fully loaded system runs approximately 45 seconds on battery power.

INT RQST L is asserted to interrupt the program if the BATTERY EMPTY or the AC LOW flags sets. The program must check the flags and determine which one caused the interrupt and what action is to be taken.

SKIP L is asserted to cause the program to skip an instruction if flag AC LOW is set or the AC LOW level is asserted and the 6102 instruction is executed or if BATTERY EMPTY is set and the 6101 instruction is executed. AC LOW flag is cleared by the 6103 instruction, but the program may still check the level by using the 6102 instruction.



* Only in slots 2 and 3 of the OMNIBUS.

Figure 6-44 Bootstrap and Auto Start Clock

6.22.3 Bootstrap and Auto-Restart Timing Clock

The bootstrap and auto-restart clock logic in Figure 6-44 generates two clock signals, CLK1 and CLK2, which provide the timing pulses for the bootstrap and auto-restart operations. The MIKP1 CLK signal is generated by a 66 kHz (approximately) RC oscillator. The clock signal is disabled by holding ENA (E65) cleared, during initialization and power up operations or when the bootstrap and auto-restart logic is in an inactive state (ACTIVE flip-flop cleared and HOLD flip-flop set). The timing for the generation of CLK1 and CLK2 is shown in Figure 6-45. CLK1 and CLK2 pulse duration is approximately 7.5 μs; both input to the JK flip-flop (E90) so that it complements on trailing edge of each clock pulse. AND gates E86A and E86B are enabled on alternate clock pulses to generate two differentclocksignals at half the frequency of the MIKP1 CLK H signal.

6.22.4 Bootstrap Initialization Logic

The purpose of this logic is to initialize the CPU, Extended Memory Control and all peripherals, preset the ROM address counter to the address selected by the bootstrap select switches, set flip-flops to provide enabling signals for the bootstrap operation, and clear the control shift register.

If S1-8 is on the bootstrap operation (Figure 6-46) is initiated when SW makes a low to high transition to clock the HOLD flip flop causing it to set. If S1-4 is on HOLD will set only if the PDP-8/A is stopped. When HOLD sets, it enables the clock (Figures 6-45 and 6-46) and clears INIT GO. The first CLK1 pulse after HOLD is set, sets flip-flop A and B which enables AND gate E64. The high out of E64 turns Q1 on and the POWER OK H line is pulled low. Asserting POWER OK H allows the CPU to negate INITIALIZE H after 200 to 1000 ms. The negation of INITIALIZE H and having cleared flip-flop A sets INIT GO.

The next CLK pulse after flip-flop A is cleared clears flip-flop B, which sets the GO flip-flop. If S1-7 is open, NAND gate E60 is enabled when go sets to assert MIKP1 ENA BOOT ADD L. This enables the address selected by the bootstrap switches to preset the ROM address counters to the address of the first ROM location to be accessed during the bootstrap operation Paragraph 6.21.3). The address is loaded into the address counter by the assertion of MIKP1 ADD LOAD L during the next CLK2 pulse. ROM A SET is not cleared until ACT is set by the next CLK1 pulse so NAND gate E54 is enabled.

The next CLK1 pulse sets ACT, which in turn clears ROM A set and allows IDLE to clear on the next CLK1 pulse. ROM A is held cleared to disable NAND gate E54 and hold MIKP1 LOAD ADD L high to remove the input from the bootstrap select switches to the ROM address counters. At this time, the ROM address counters are preset to the address of the first ROM location to be accessed.

At this point, control of the bootstrap operation is taken over by the four control bits out of ROM No. 1 control counter (Paragraph 6.21.3).

6.22.5 Auto-Restart Initialization Logic

The purpose of this logic is to Initialize the CPU, the Extended Memory Control and all peripherals, preset the ROM Address counter to the address selected by the auto-restart switches, set the necessary flip-flops to provide enabling signals for the auto-restart operation, and clear the control shift register (Figure 6-47).

An auto-restart operation is initiated when AC LOW L is negated after power is turned on. The initialization and conditioning of the logic to enable an auto-restart operation is similar to the bootstrap operation so this description will not be repeated.

Having disabled NAND gate E54, and not running the CPU enables the data input to the AR flip-flop, and when AC LOW L is negated (high) the AR flip-flop sets. If S1-6 and S1-7 are ON (closed) the MIKP1 ENABLE RESTART ADD L is asserted to apply the address selected by the auto-restart switches to the address counter input. ROM A set is dc set by having cleared ACT during the initialization during power up. NAND gate E54 is enabled by CLK2 and MIKP1 ADD LOAD L presets the address counter with the address selected by the auto-restart switches. ROM A is cleared, and the next CLK2 pulse after IDLE is cleared as it was for the bootstrap operation (Paragraph 6.21.3).

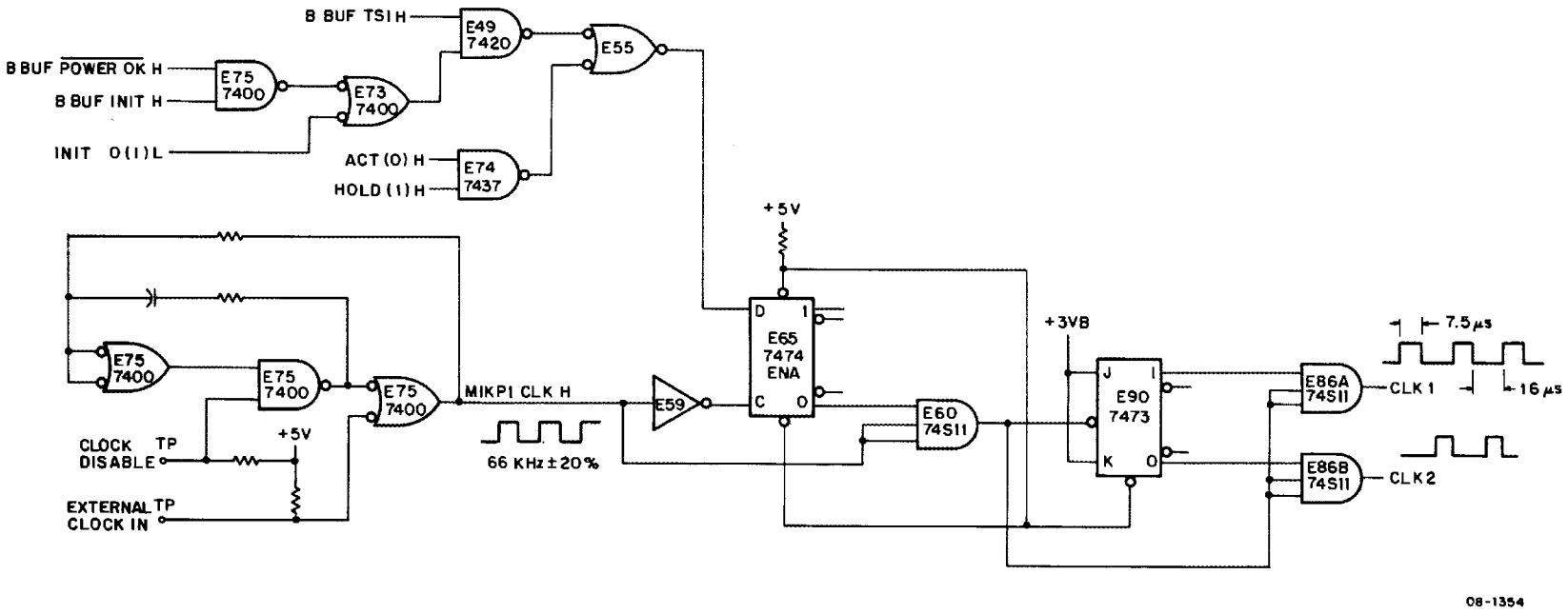


Figure 6-45 Bootstrap and Auto Start Clock

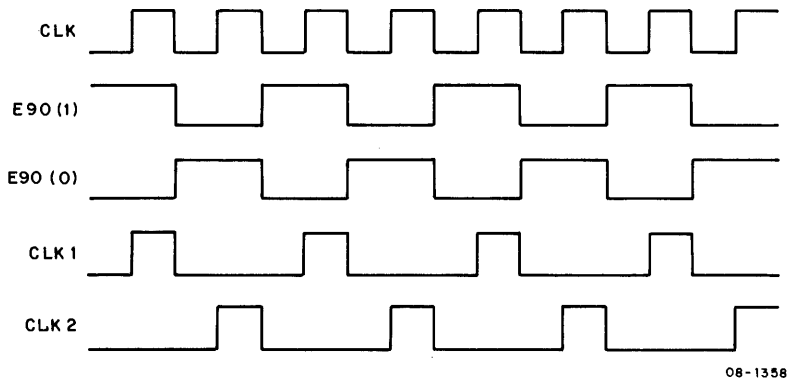


Figure 6-46 CLK1 and CLK2 Timing

6.22.6 Auto-Restart and Bootstrap Address Counters

The address counters in Figure 6-48 are preset to the first ROM address to be accessed when an auto-restart or bootstrap operation is started. The first address is always an even number. The 2 8266 IC's select either the condition of the bootstrap select switches or the auto-restart switches as input to the address counters. The address counter, consisting of two 74197 ICs is loaded when MIKP1 ADD LOAD L is asserted (see Figure 6-47). Incrementation of the counter takes place at the end of a control register cycle where CLK2 is ANDed with RECYCLE asserting MIKP1 INCRMT ADD counter L. The bootstrap and auto-restart switch settings are listed in Tables 2-10 through 2-13.

6.22.7 ROM Memory Control and Multiplexers

ROM Nos. 1 and 2, along with their associated multiplexers and control logic, are shown in Figure 6-49. The ROMs are addressed by the address counter and supply as output four control bits and a 12-bit word (Figure 6-38). The control bits are used to generate control signals which are used to load an extended memory address (field), load the memory address, or deposit a 12-bit word into read/write memory. The first 16-bit word read from memory also contains a bit which asserts MIKP2 START H. This signal is used to assert INITIALIZE H (Figure 6-49) during the first pass through the control shift register, and initialize the CPU, extended memory option, and all peripherals. The content of the two addressed locations in ROM Nos. 1 and 2 are transferred to the Data Bus during TS2 for deposit operations or by MIKP2 ENA DATA H to load the extended address or memory address.

MIKP2 ENA ADD DATA H is asserted by outputs of the control shift register (Figure 6-50) to enable the address data.

6.22.8 Bootstrap and Auto-Restart Operation Control Logic

The function of the control shift register and the associated logic is to assert the Omnibus signals required to address memory deposit information in a memory location and start the program. During auto-restart operations, a memory address is loaded into the memory address register and the program is started in field 0 at the selected address.

The control shift register is a 74164 IC used as an 8-bit shift register. A high on the two serial inputs allows the first bit to become a one on the first CLK1 pulse after ROM A sets. Subsequent clock 1 pulses will shift the 1 through the shift register and as it is shifted, the control signals on the output are asserted to assert the necessary Omnibus and control signals for the bootstrap and auto-restart operations. The timing required for these operations is shown in Figures 6-43 and 6-44. In subsequent passes the bit 1 in the shift register is set to 1 by RECYCLE out of the shift register.

A description of the Omnibus signal, asserted by the control signals out of the control shift register, is in Chapter 3.

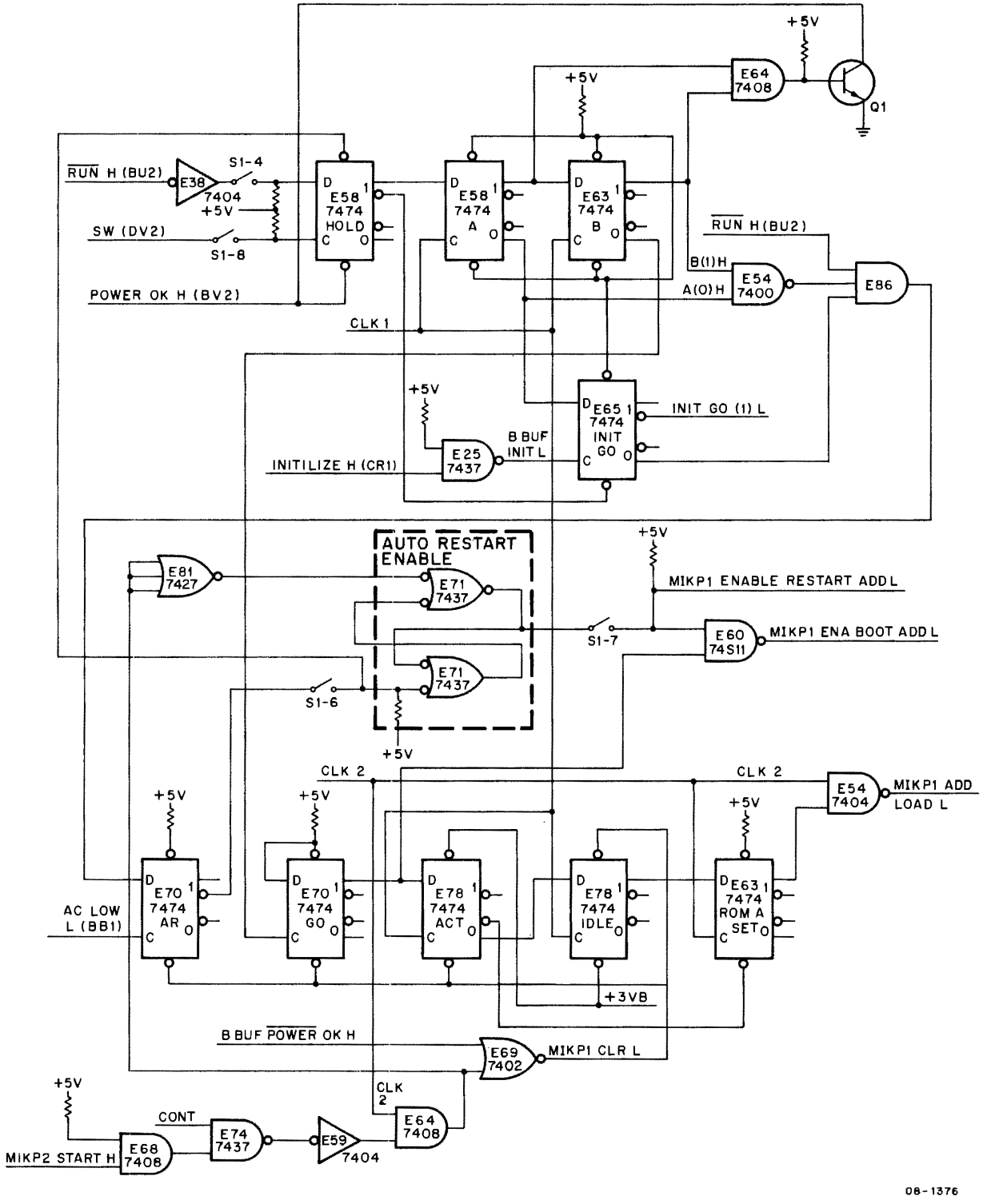


Figure 6-47 Auto Restart Initialization Logic

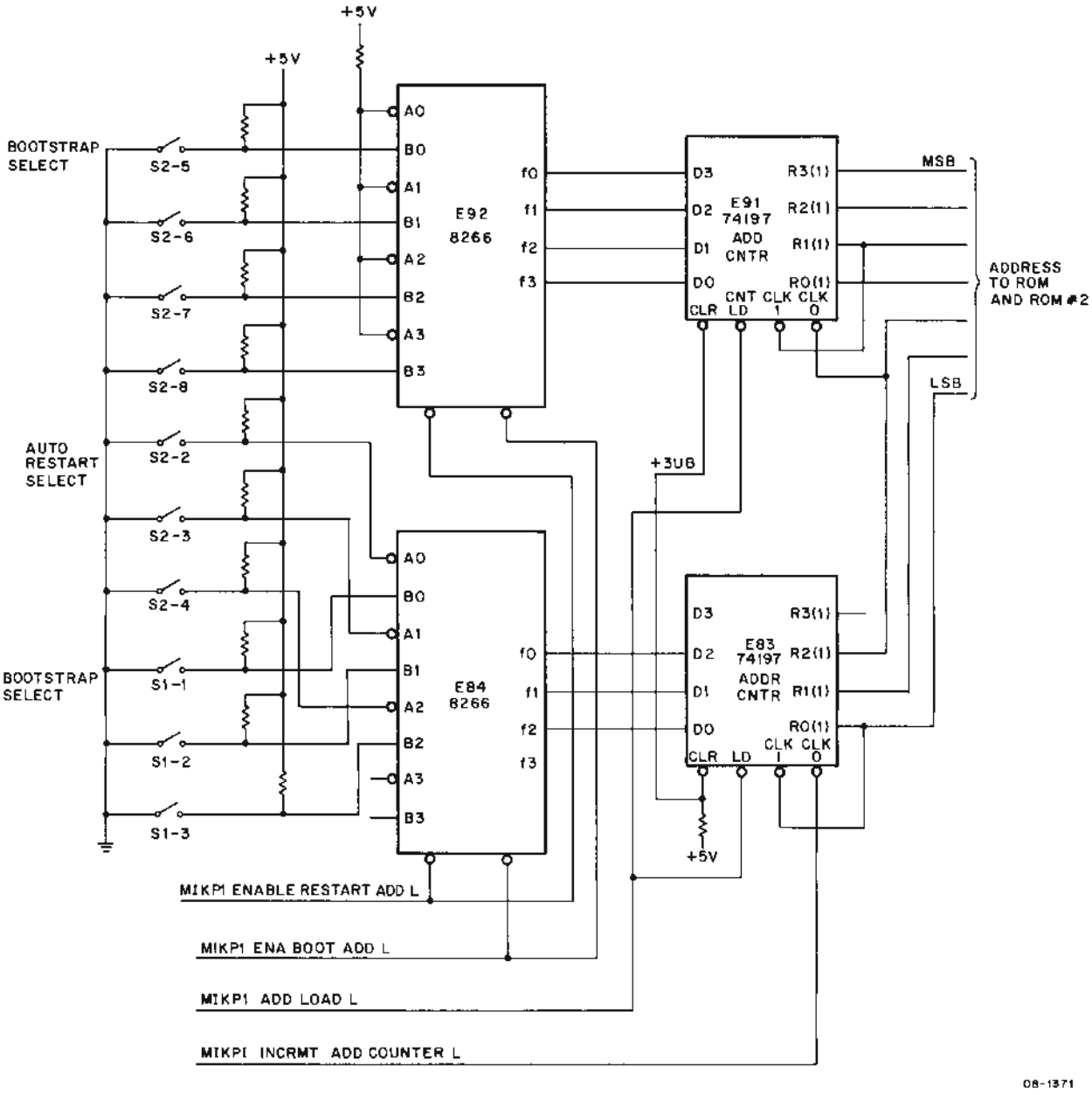


Figure 6-48 Auto Restart and Bootstrap ROM Address Counters

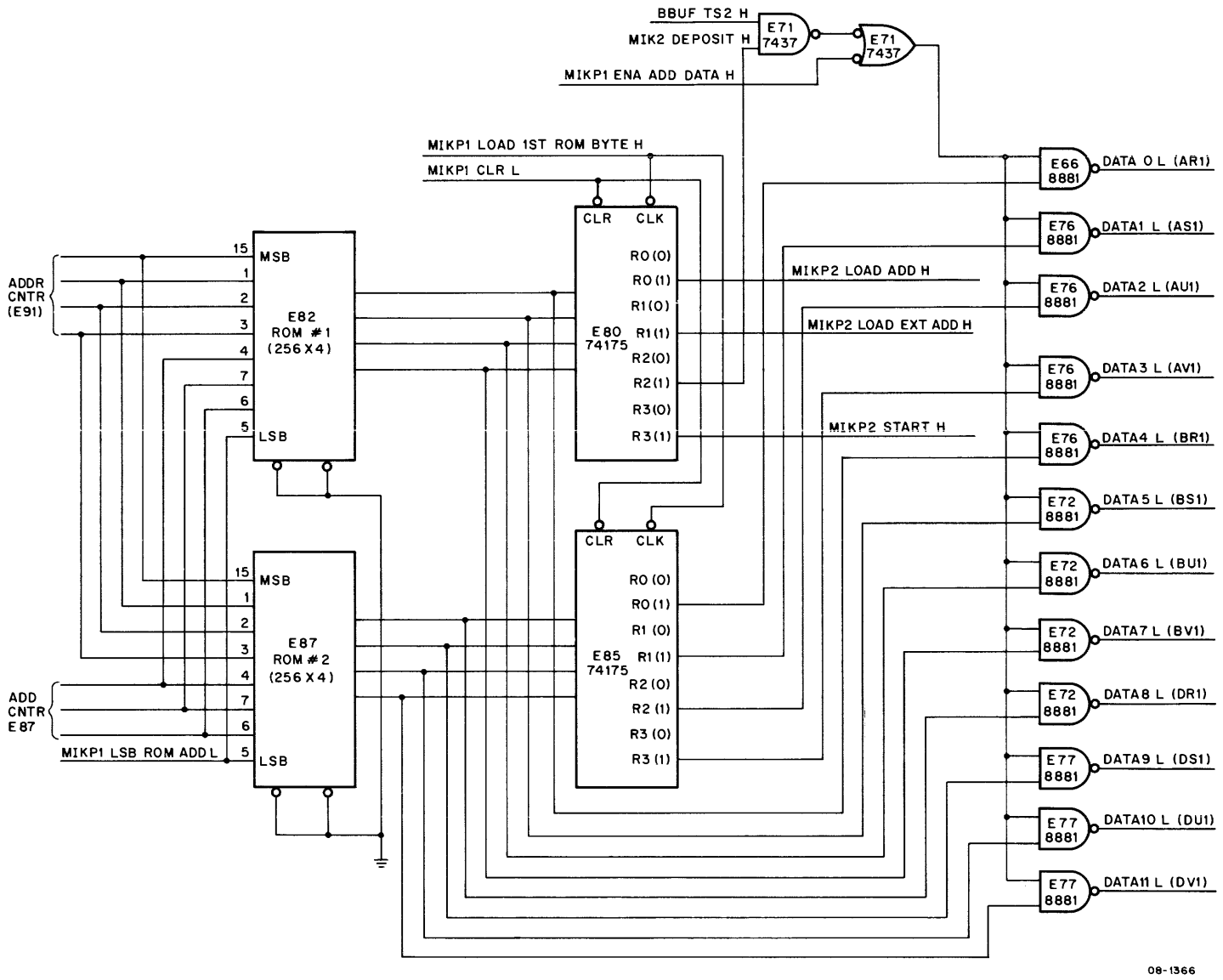


Figure 6-49 ROM Memory Control and MUX

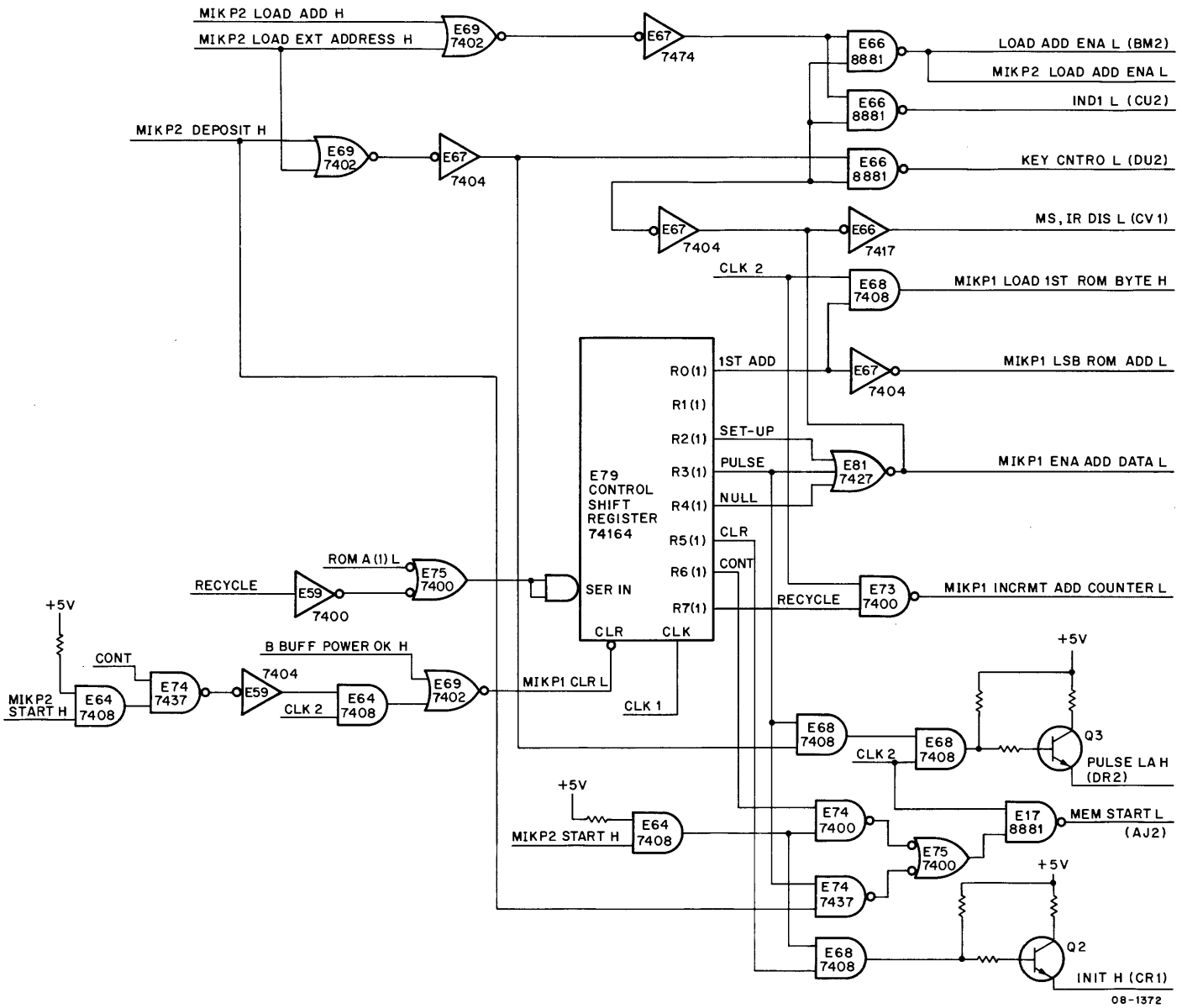


Figure 6-50 Bootstrap and Auto Restart Operation Control Logic