2

system introduction

PDP-8/E BASIC SYSTEM

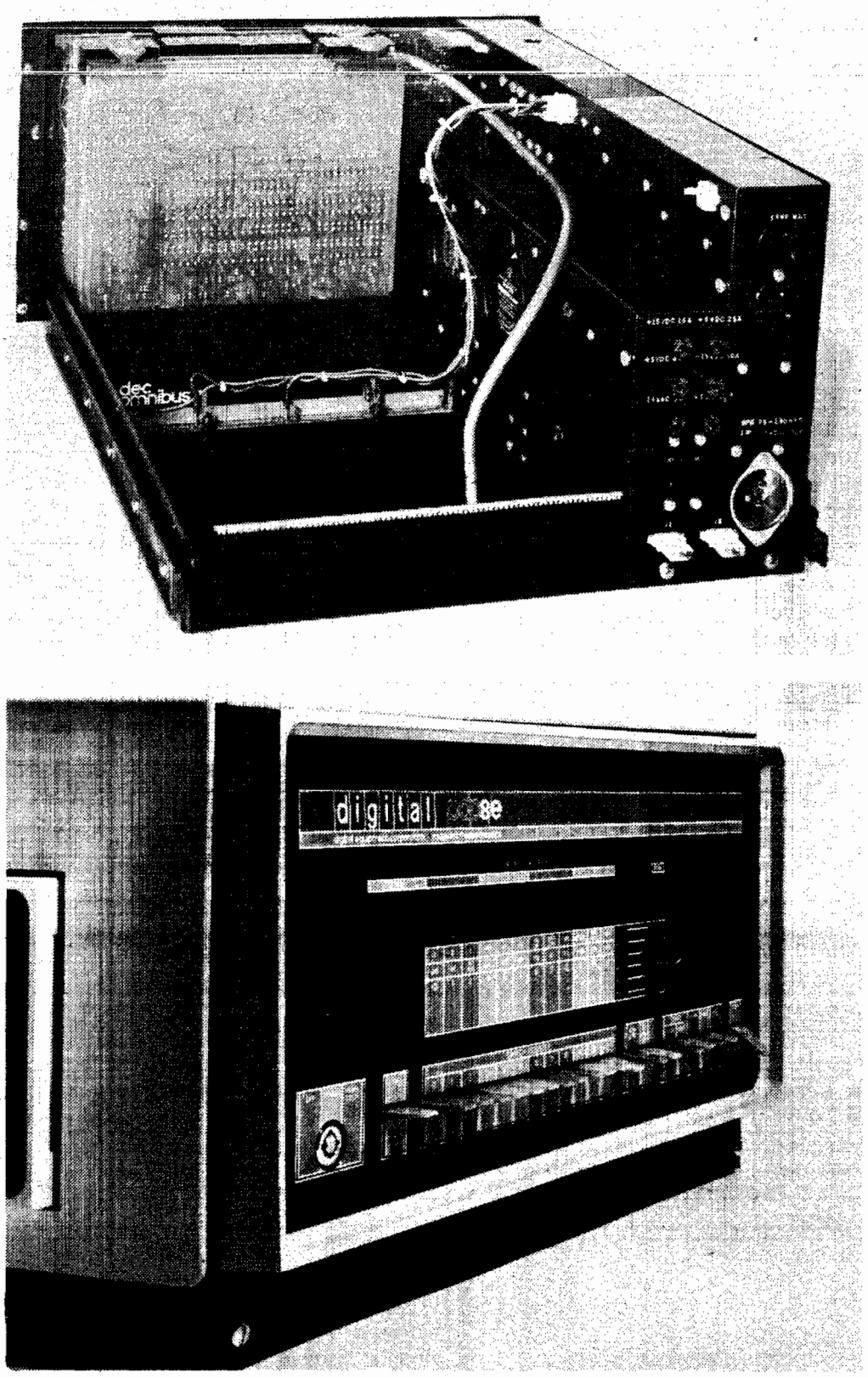
The PDP-8/E is specially designed as a general purpose computer. Its development is the successful culmination of many years of computer design research directed toward providing better computers at the lowest possible price. The PDP-8/E is designed to meet the needs of the average user, yet it is capable of modular expansion to accommodate almost any requirements for a user's specific application.

The PDP-8/E basic processor is a single-address, fixed word length, parallel transfer computer using 12-bit, two's complement arithmetic. The cycle time of the random access memory is 1.2 microseconds for fetch and defer cycles without autoindexing and 1.4 microseconds for all other cycles. Standard features include indirect addressing and facilities for instruction and skipping and program interrupts as a function of input/output device conditions.

Five 12-bit registers are used to control computer operations, address memory, perform arithmetic or logical operations and store data. A programmer's console provides switches and indicators that permit convenient monitoring and modification of machine states and major registers. The PDP-8/E may be programmed manually, using the programmer's console, or remotely, by means of a console terminal.

The 1.2/1.4 microsecond cycle time of the PDP-8/E provides a computation rate of 385,000 additions per second. Each addition requires 2.6 microseconds (with the addend in the accumulator), while subtraction requires 5.0 microseconds (with the subtrahend in the accumulator). Multiplication is performed in 256.5 microseconds or less by a subroutine that operates on two-signed, 12-bit numbers to produce a 24-bit product, leaving the 12 most significant bits in the accumulator. Division of the two signed, 12-bit numbers is performed in 342.4 microseconds or less by a subroutine that produces a 12-bit quotient in the accumulator and a 12-bit remainder in memory. Similar signed multiplication and division operations are performed in approximately 40 microseconds utilizing the optional KE8-E Extended Arithmetic Element.

The flexible, high capacity input/output capabilities of the PDP-8/E allow it to operate a variety of peripheral devices. Besides a choice of console terminals, the PDP-8/E supports more than 60 input/output device options including high-speed paper tape equipment, card readers, line printers, disk and magnetic tape bulk storage devices and a wide range of data acquisition, transmission and display peripherals.



PDP-8/E Programmed Data Processor
(Table-top Model)

Every PDP-8/E system is completely self-contained. A single source of 115 or 230 volt AC power is required; however, internal power supplies produce all necessary operating voltages for the system. Rack mounted computers are supplied with standard cabinets that are large enough to accommodate the PDP-8/E and several peripherals in less than 5 square feet (0.5 square meters) of floor space. The table top version is a convenient alternative for users who plan to install the computer in a confined area, such as an office. The table top PDP-8/E weighs only 100 pounds (45 kilograms) and displaces less than 3 cubic feet (0.8 cubic meters).

The basic PDP-8/E computer consists of a table top or rack mounted cabinet with an H274 (or H274-A) power supply, and an OMNIBUS on which the KK8-E Central Processor, memory system, programmer's console and console terminal control are mounted. In the PDP-8/E, a bus is defined as a group of 12 signal lines carrying related information, such as the 12 bits of an instruction or data word. The OMNIBUS may be considered as a wide bus containing several busses, along with many other signal lines. Each OMNIBUS contains 20 identical, non-dedicated module slots, and each slot will accept a 144-pin QUAD-size module. The OMNIBUS provides a two-way signal path between corresponding pins of the modules that are plugged into it.

The PDP-8E central processor consists of five QUAD modules that plug directly into the OMNIBUS. The memory system is contained on an additional three QUAD modules, while the programmer's console and console terminal control occupy one module each. Figure 2-1 is a block diagram of the basic PDP-8/E that illustrates the signal paths between the central processor, the memory system and the OMNIBUS. Signals that do not pass through the OMNIBUS are routed between adjacent modules by means of H851 Edge Connectors.

KK8-E CENTRAL PROCESSING UNIT

The KK8-E Central Processor consists of the major registers module, major registers control module, timing generator, bus loads module and RFI shield. These five functional units contain most of the timing and gating circuitry used to manipulate data and generate control signals.

M3800 MAJOR REGISTERS MODULE

The major registers module contains five special purpose registers that are used in almost every programming application, as well as additional gating circuits and a 12-bit parallel adder. These components are described separately in the following paragraphs.

Accumulator (AC)

The accumulator, or AC, is a 12-bit register in which arithmetic and logical operations are performed. The accumulator may be cleared, complemented or incremented under program control, and its contents may be rotated right or left. The content of the memory buffer register may be combined with the content of the AC by two's complement addition or by a bitwise logical AND operation. The content of the programmer's console switch register may be combined with the content of the AC by a bitwise logical OR operation. In every case, the result is left in the AC.

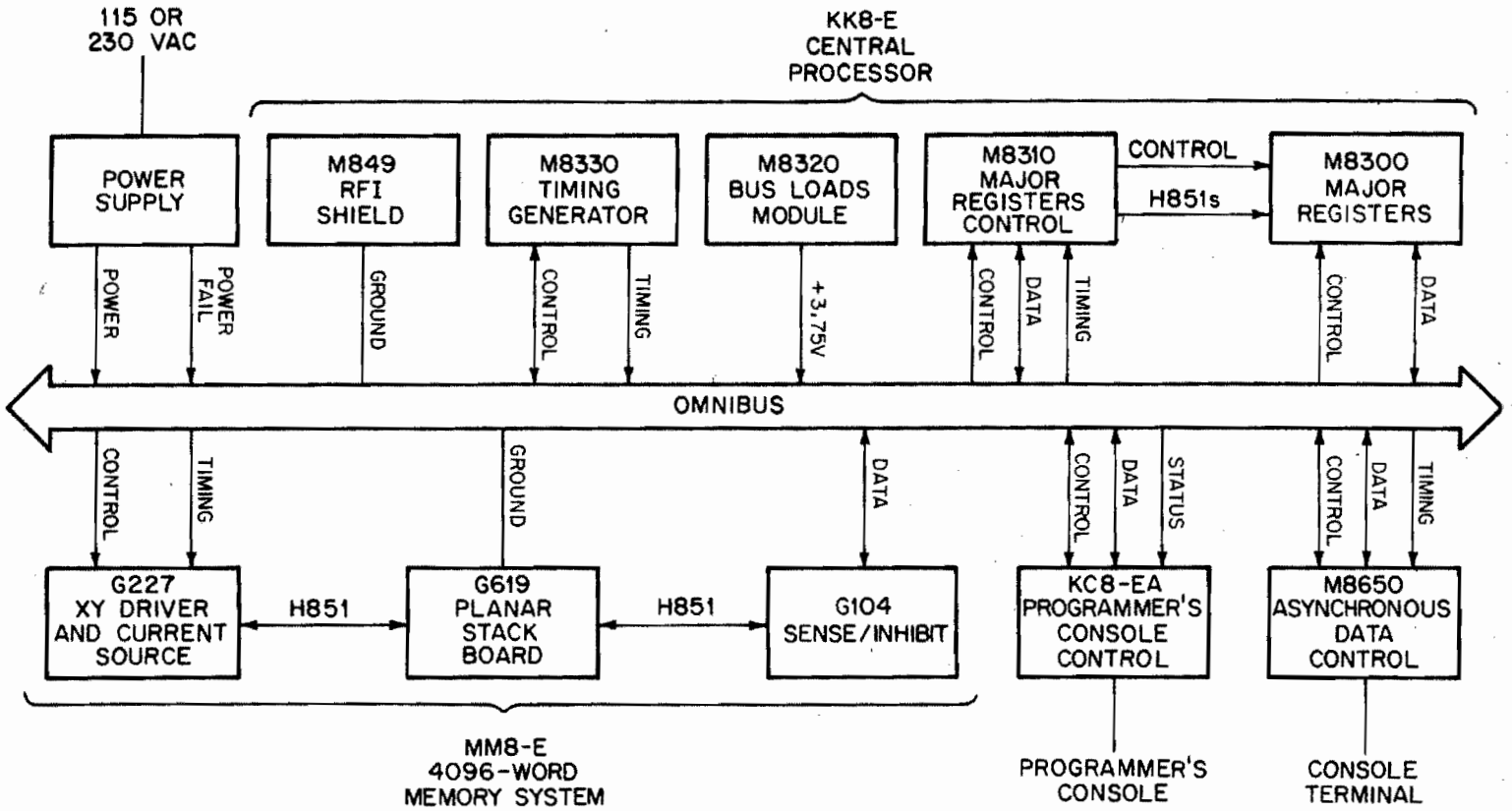


Figure 2-1 PDP-8/E Basic System Block Diagram

The AC may also serve as an input/output register. All programmed data transfers between memory and I/O devices pass through the AC to data lines located on the OMNIBUS. I/O transfers performed via data breaks, or direct memory access, do not pass through the AC, however.

Multiplier Quotient Register (MQ)
The multiplier quotient registers, or MQ, is a 12-bit bidirectional shift register that acts as an extension of the AC during extended arithmetic operations. When a KE8-E Extended Arithmetic Element is installed, the MQ contains the multiplier at the beginning of a multiplication and the least significant half of the product at the conclusion. It contains the least significant half of the dividend at the start of a division and the quotient at the conclusion, or the least significant part of a number during shift and normalize operations. The MQ is available as a temporary storage register, even if a KE8-E is not installed.

Program Counter (PC)
The program counter, or PC, is a 12-bit register that contains the address of the memory location from which the next instruction will be taken. The PC is automatically incremented by 1 after each instruction is read from memory. It may be incremented under program control, to conditionally skip the next sequential instruction, or loaded from the memory buffer register, to cause a programmed jump to a prescribed memory location.

Central Processor Memory Address Register (CPMA)
The CPMA is a 12-bit register that contains the memory address currently selected for reading or writing. This register is never cleared; information is always jam transferred in and the original content is lost. The CPMA may be loaded from the memory buffer register, the program counter or the programmer's console switch register. Extended memory and data break interfaces provide additional memory addressing capabilities.

Memory Buffer Register (MB)
The MB is a 12-bit register through which all information is transferred between the central processor registers and memory. Data may be read into the MB from any memory location in 0.6 microseconds and rewritten at the same location in another 0.6 microseconds. The content of any location may be read, incremented, tested and rewritten in the same location in a total of 3.8 microseconds or less. The MB may be loaded from either the AC, the PC or memory.

Data Gates and Adders
The major registers module also contains the gating circuitry necessary to move data from one register to another. At the heart of the data gating circuitry is a 12-bit parallel adder. Information from a register is gated to the adder inputs. The output of the adder is applied to a set of shift gates, and the output of the shift gates serves as data input to all of the major registers.

M8310 MAJOR REGISTERS CONTROL MODULE

The major registers control module contains the link, the major register control circuits, the major state generator and the instruction register, as well as additional miscellaneous control circuits. This circuitry is responsible for the actual decoding and execution of most PDP-8/E instructions. Control signals are transmitted between the major registers control module and the major registers module by means of two H851 Edge Connectors. Important components of the major registers control module are described separately in the following paragraphs.

Link (L)

The link is a 1-bit register that serves as a high-order extension of the AC. It is used as a carry register for two's complement arithmetic. The link may be set, cleared or complemented under program control. At the same time, it may also be rotated left or right as part of the accumulator.

Major Register Control Circuits

The major register control circuits gate timing, data and control signals to enable the adder input and shift gates of the major registers module. They also gate timing pulses that regulate data transfers to and from the major registers.

Major State Generator

The major state generator determines which of three major states the central processor is about to enter. Each major state corresponds to a signal that is asserted to enable the appropriate register control circuitry. A fourth major state is entered when none of the signals produced by the major state generator are asserted. Specifying one of the four major states determines which data gating circuits will be enabled during a given memory cycle.

Instruction Register (IR)

The IR is a 3-bit register that contains the operation code of the instruction that is currently being executed. The three most significant bits of each instruction are loaded into the IR after the instruction is read from memory. This data is decoded and used to determine which major states will be entered during instruction execution.

M8320 BUS LOADS MODULE

The bus loads module receives +5 and +15 volt inputs from the power supply and provides +3.75 volt (voltage level high) output to load the OMNIBUS signal lines. Most signal lines are considered to be inactive until the voltage level is pulled to ground by a component that is asserting the line.

M8330 TIMING GENERATOR MODULE

The timing generator module contains the time pulse generator, interrupt control circuits, the processor input/output transfer instruction decoder and other miscellaneous control circuits.

The time pulse generator provides four time states, designated TS1 through TS4, and four time pulses, designated TP1 through TP4. Each time pulse overlaps the end of one time state and the beginning of the

following time state. The time states are used to initiate squential, time-synchronized gating operations. The time pulses are used for memory timing and as gating pulses throughout the system. In addition, the power clear pulse generator produces pulses that reset registers and control circuits during power turn-on and turn-off. Several of these pulses are available for the control of peripheral devices.

The interrupt control circuits comprise the major portion of the interrupt system. This circuitry responds whenever an interrupt request signal is received from an interface controller module. Processor input/output transfer instructions are used to initialize and operate the interrupt system under program control.

M849 RFI SHIELD MODULE

The radio frequency interferences (RFI) shield module ensures that signals which are not synchronized with memory do not interfere with the memory circuits. Aside from a ground path, the RFI shield has no important connections to or from the OMNIBUS.

KC8-EA PROGRAMMER'S CONSOLE

The programmer's console module contains the circuitry required to operate the PDP-8/E programmer's console. This console consists of an array of controls and indicators that facilitate computer operation and maintenance. Twenty-two switches provide convenient control of the system by allowing the operator to start and stop program execution, examine and modify the content of memory, select various modes of operation, or load and execute short machine language programs.

A 6-position rotary switch selects one of six registers or groups of registers for display in 12 bits of the 28-lamp indicator panel. A lighted indicator lamp indicates the presence of a binary 1 in the specified bit position of a register or control flip-flop. The 15-bit address of the memory location being accessed and the state of the RUN flip-flop are displayed at all times.

A 3-position key operated switch permits the computer to be locked in a power off state, a power on state with all switches and indicators activated, or a power on state with only the SW switch and RUN indicator activated. This feature serves to protect a running program from inadvertent switch or control operation.

M8650 ASYNCHRONOUS DATA CONTROL MODULE

The KL8-E Asynchronous Data Control, consisting of one M8650 module, contains the receive, transmit and control circuitry needed to interface an LT33 or LT35 Teletype terminal, VT05 DECterminal, or any similar asynchronous device with the central processor. This module serves as a serial-to-parallel converter for transmitting input signals, or a parallel-to-serial converter for transmitting output signals. It also performs certain control functions such as instruction skipping as a function of terminal condition and transfer of program control via program interrupt.

Eight models of the KL8-E provide a variety of transmit/receive rates ranging from 110 baud to 1200 baud. The 110 baud model is available with a choice of cabling for EIA/CCITT or 20 mA operation, while all