CHAPTER 3
PRINCIPLES OF OPERATION

3.1 INTRODUCTION

This chapter presents three levels of PDP-8/E System operation. First, a simplified block diagram presenting the primary parts of the processor is discussed. Second, a flow chart relating the processor instructions to time states is presented and discussed with appropriate references to the corresponding third-level discussion. The third-level discussion presents the logic theory and is divided into functional groups of logic. A reference to the modules is provided so that continuity between the principles of operation and the engineering drawings exists throughout the discussion.

NOTE

The component designations are for reference only and do not necessarily correspond to those designations on engineering drawings.

Chapter 3 is divided into eight functional sections:

Section 1 – System Introduction

Section 2 – System Flow Diagrams

Section 3 – Timing Generator

Section 4 – Memory System

Section 5 – Central Processor

Section 6 – I/O Transfer Logic

Section 7 – Teletype Control

Section 8 – Power Supply

This format is provided to aid the user in understanding the principles of operation and to distinguish the individual parts of the basic PDP-8/E processor.

3.2 PDP-8/E BASIC SYSTEM

The PDP-8/E processor contains eight functional areas and can accommodate as many as 60 options. A simplified block diagram, Figure 3-1, relates the OMNIBUS to the major signals and the eight functional areas. Each of the functional areas is contained on a single quad-size module with the exception of the MM8-E (three modules are provided).

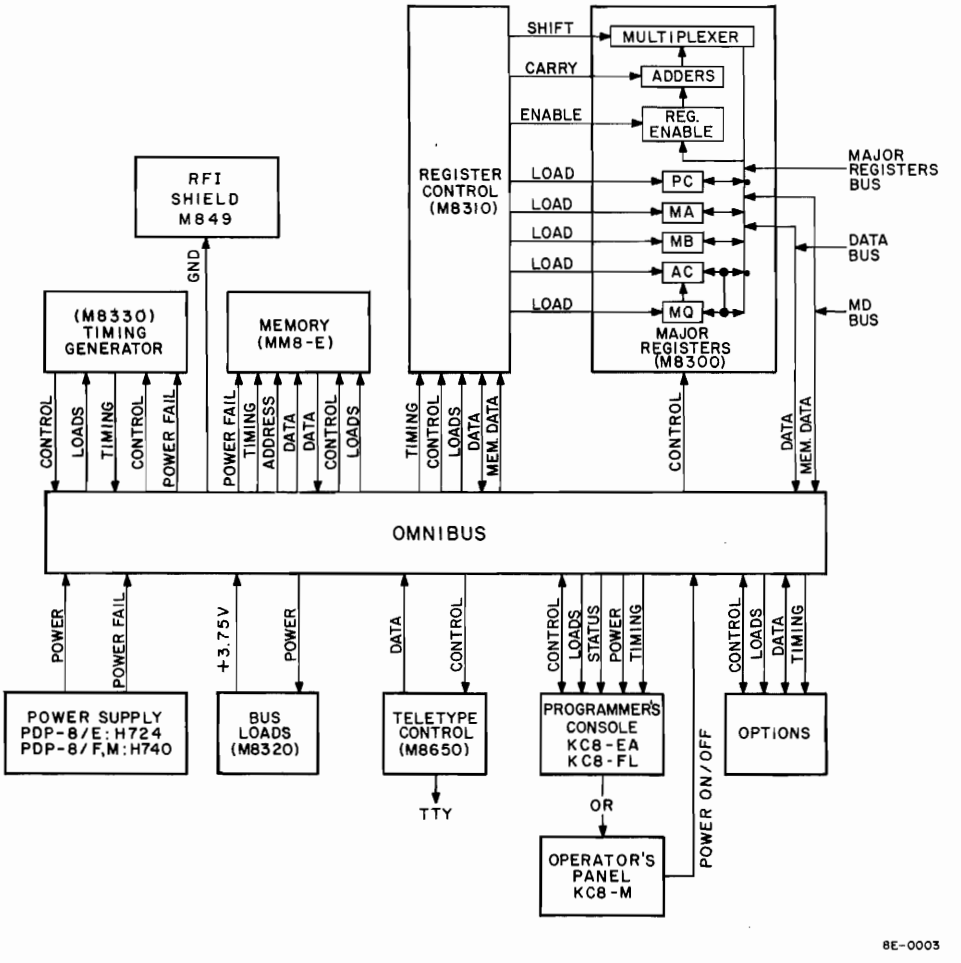

Figure 3-1 PDP-8/E Simplified Block Diagram

3.2.1 OMNIBUS

The OMNIBUS provides a two-way path between the corresponding connector pins of the modules that plug into it. To accommodate 96 signal lines plus ground and power at the module connectors, 144 pins are provided. In general, each signal line is kept at a +3.75 Vdc level and pulled to ground when the signal is asserted. However, exceptions occur, with respect to power levels and some timing and control signals. Bus loads provide this capability by applying +3.75 Vdc to the bus lines via load resistors. When a signal line is asserted, the output driver of that signal pulls the line to ground, the corresponding input circuits (on the same module or a different

module) are activated due to the low signal. This technique facilitates the interaction between modules and makes it possible to connect many modules to the same bus. Some signals do not use the OMNIBUS. The connection of the M8310 Register Control module and the M8300 Major Registers module is partially accomplished using an H851 Edge Connector for all of the control signals. Data is exchanged through the OMNIBUS.

3.2.2 Timing Generator (M8330)

The timing generator provides four time states (TS1 through TS4), four time pulses (TP1 through TP4) and memory timing signals. One memory cycle is accomplished between TS1 and TS4. A choice of two memory cycles is provided: a slow (1.4 μs) and a fast (1.2 μs) cycle. Control inputs are provided by the register control module and the power supply.

3.2.3 Memory (MM8-E)

Three memory modules are provided: the G619 Memory Stack, the G227 X/Y Driver and Current Source, and the G104 Sense/Inhibit.

The memory stack contains 12 core mats, each consisting of 4096 cores and selection diodes to provide a 12 bit-per-word, 4096 word storage capability.

The X/Y driver and current source module contains the selection switches, drivers, and current source required to fully select any one of the 4096 memory locations.

The sense/inhibit module is used to sense (read) any one of the 4096 memory locations and to write into any memory location.

3.2.4 Register Control (M8310)

The register control has many functional logic circuits that generate the major states of the processor, determine the instruction to be performed, and control the operation of the major registers (M8300). The register control receives a word from memory, decodes the word, and determines the operation to be performed. Functional logic is provided to gate bits into the major register adder circuit, shift right, or shift left. The M8310 develops register transfer signals and register load signals. The timing generator determines when these signals are generated.

3.2.5 Major Registers (M8300)

The major registers module provides the Program Counter (PC) Register, the Central Processor Memory Address (CPMA) Register, the Memory Buffer (MB) Register, the Accumulator (AC) Register, and the Multiply-Quotient (MQ) Register. Transfer of information in the AC to the MQ is accomplished directly through enabling logic. Transfer of all other registers is accomplished through the register enable logic, through the adders, and through the output multiplexers, where the information is placed onto the MAJOR REGISTERS BUS. Information can be brought into the MAJOR REGISTERS BUS from the DATA BUS and the MD BUS or transferred out to the same lines. Transfer of MB data to the MD lines is accomplished by MD DIR (H).

3.2.6 Power Supply (H724)

The power supply receives an input of 95 to 130 Vac, 47 to 63 Hz and provides 28 Vac, +8 Vdc, +5 Vdc, -15 Vdc, and +15 Vdc to the PDP-8/E System. The power system is interlocked with the front panel key switch. Power fail and overload detection are provided to ensure the protection of system components and system performance.

3.2.7 Bus Loads (M8320)

The bus loads receive +5 Vdc and +15 Vdc inputs from the power supply and provide a +3.75 Vdc output to the signal lines on the OMNIBUS.

3.2.8 Teletype Control (M8650)

The Teletype control module contains a receive register and transmit register, decoders, and interprets two flags. It performs the conversion of parallel computer words to serial Teletype words, assembles serial Teletype characters into data words for the computer and commands from the computer.

3.2.9 Programmer's Console (KC8-EA)

The programmer's console is a plug-in module, containing logic, lamps, and switches. The face panel, which contains openings for the switch levers and a silk-screened switch/indicator identification, is mounted in front of the programmer's console module. The panel OFF/POWER/PANEL LOCK switch is controlled by a key. The programmer's console enables the operator to deposit a 12-bit word into memory, read any memory location, observe the content of important registers, read the instruction currently being processed, and observe every primary activity the processor is currently performing.

3.2.10 RFI Shield (M849)

The RFI shield module ensures no interference of memory circuits with nonmemory options (those options not synchronized with memory).

3.2.11 Options

More than 60 options are available to the PDP-8/E user. The one option described in this volume is the Teletype control option. All other internal bus options are described in Volume 2. External bus options are described in Volume 3.

3.2.12 Signal Finder

The basic PDP-8/E signals and their descriptions are given in Table 3-1. If the reader desires to study the detailed logic as he is progressing through the flow diagrams, a corresponding paragraph reference to the detailed logic is provided. Refer to Appendix B for source-destination module designations.

Table 3-1
Signal Finder

Signal Name	Logic Reference	Signal Description
DATA T DATA F	3.35.3	Data Control GATE ENABLING signals – DATA BUS TO ADDERS: DATA T, DATA F COMPLEMENT OF DATA BUS TO ADDERS: DATA T, DATA F ZERO TO ADDERS: DATA T, DATA F*
AC → BUS L	3.35.2	Enables the Data Line MUX to allow the contents of the AC to be applied to the DATA BUS.
MQ → BUS L	3.35.2	Enables the Data Line MUX to allow the contents of the MQ to be applied to the DATA BUS.
SHL + LD ENA L AC → MQ ENA L	3.40	Enable signals applied to the MQ MUX to output either the MQ (one place to the left) or the contents of the AC. **SHL + LD ENA L / AC → MQ ENA L / Output** L / L / MQ (left) L / H / MQ (left) H / L / AC H / H / 0
F SET L D SET L E SET L	3.34.1	Indicates the next major state. For example, F SET L means that the next major state is FETCH.
F L, D L, E L	3.34.1	Indicates the current major state.
DMA	3.8	Direct Memory Access State – asserted when MS, IR DISABLE is grounded.
INT IN PROG	3.42.1	Interrupt in Progress – this signal acknowledges an interrupt request and forces a JMS to the IR and EXECUTE to the Major State Register.
INT REQUEST L	3.42.1	Interrupt Request – when asserted (low) means that a device has set a flag and is requesting an Interrupt.
USER MODE	3.42.1	Used with the time-sharing option to prevent programmed halt, I/O PAUSE, OSR, or LAS.

*This condition cannot exist during OPERATE and TS3.

Table 3-1 (Cont)
Signal Finder

Signal Name	Logic Reference	Signal Description
INT BUS L	3.33.1.2 3.33.2.2	When the programmer's console STATUS switch is in STATUS, an INT REQUEST occurs, and the INT BUS indicator is illuminated.
LOAD, AC MQ MB CPMA PC	3.37	When data is to be placed into one of the Major Registers, the corresponding load signal is developed.
INT STROBE	3.41	Interrupt Strobe – Developed by BUS STROBE and NOT LAST XFER or TP3 to set the INTERRUPT SYNC flip-flop. Used by the interrupt and break systems.
I/O PAUSE L	3.41.2	Signifies that an IOT is being processed. It is used by the peripheral control modules to gate device selectors and to gate data onto the DATA BUS. This signal is used to initiate OUTPUT transfers; in the central processor, it is used to control IOT decoding.
BUS STROBE L	3.41.2	BUS STROBE L is used for IOT instructions to load data into the AC or PC and, with NOT LAST XFER L, generates INTERRUPT STROBE.
INTERNAL I/O L	3.41.4	Used to inhibit the generation of IOPS by the positive I/O bus interface.
C0 L, C1 L, C2 L	3.41.1	Controls the type of I/O data transfer between a device and the processor.
MS, IR DISABLE L	3.34	Major State, Instruction Register Disable – Used during Direct Memory Access to disable FETCH, DEFER, or EXECUTE major state and instruction register.
KEY CONT L	3.33.1.1	Key Control – A control signal developed in the front panel logic.
STOP L	3.16	Stop resets the RUN flip-flop and causes timing to halt at TS1.
CONT	3.33.1.1	Continue – A front panel key to force the processor into automatic timing.
ADDR LOAD L	3.33.1.1	Address Load – A front panel key used to manually load an address into the CPMA.

Table 3-1 (Cont)
Signal Finder

Signal Name	Logic Reference	Signal Description
EXTD ADDR L	3.33.1.1	Extended Address Load – A front panel key used to manually load the address of extended memory.
DATA 0–11 L		The DATA BUS containing 12 bits of information.
FIELD	3.27.4	Corresponds to extended memory up to 32K as follows: BASIC MEMORY: FIELD 0 EXTENDED MEMORY: FIELD 1 – FIELD 7
NOT LAST XFER L	3.41.2	Used primarily with the device on the positive I/O bus, requiring more than 1.2 μs to perform an IOT.
BRK DATA CONT L	3.8.2 and 3.33.1.1	Used to gate the contents of the MD BUS through the Register Input Multiplexer.
EN0 EN1 EN2	3.35.1	Register Input Multiplexer enabling signals to allow the contents of the Major Registers to be placed into the ADDERS.
OVERFLOW L	3.39	Overflow – Occurs when carry-out is asserted from adder state 0 at TP2.
CAR OUT L	3.39	Carry Out – Asserted when 7777_8 is incremented by 1 in the adder.
CAR IN L	3.36.1	Carry In – Developed to add a 1 to a register.
SKIP L	3.38	The output of the SKIP flip-flop is applied to carry-in logic. SKIP is set during a variety of conditions such as OVERFLOW during an ISZ instruction and programmed microinstructions (GROUP 2).
SHIFT– LEFT L RIGHT L TWICE L NO SHIFT L	3.36.2	Shift Signals that cause the adder output multiplexer to shift left, or right, or twice left or twice right, or byte swap.
PAGE Z L	3.36.2	Asserted when Page Zero is to be addressed. PAGE Z is applied to the adder output multiplexer to apply zeros to CPMA0-4.

Table 3-1 (Cont)
Signal Finder

Signal Name	Logic Reference	Signal Description
MD DIR L	3.28	Memory Data Direction – Used to control memory data during the read and write operation. MD DIR L: Places the contents of the MEM REG on the MD BUS. MD DIR: Places the contents of the MB Register on the MD BUS.
DEP	3.33.1.1	Deposit – A front panel key used to manually load information into memory.

3.3 DATA PATHS

Because the OMNIBUS concept is different from other PDP-8 family processors, the reader should understand the relationship of the data paths to the OMNIBUS.

The OMNIBUS should be considered a bus containing several buses. A bus is defined as a group of 12 signal lines, carrying information. With this definition, the PDP-8/E contains the MEMORY DATA (MD) BUS, the DATA BUS, the MEMORY ADDRESS (MA) BUS, and the MAJOR REGISTER BUS. All buses (except MAJOR REGISTER BUS) are on the OMNIBUS. The OMNIBUS also contains the transfer control signals for I/O operations.

Data paths are illustrated in Figure 3-2. Although the illustration does not show all of the signals on the OMNIBUS, it is obvious from the data paths that signal origins and destinations appear in many places. Using the MD BUS as an example, memory data is provided by the Memory Register, the MB Register, and memory options. The MA BUS receives the memory address from the CPMA Register and from some options that generate the 12 address bits. The MA BUS applies these 12 bits to the XY selection decoder of the memory. The DATA BUS is used to receive Switch Register data, provide status to the Programmer's Console, carry information to and from a peripheral or internal option, and provide a path for data to the MAJOR REGISTERS BUS.

The MAJOR REGISTERS BUS completes a return path to each of the major registers. The CPU controls inputs to the major registers, and the enabling logic causes operations such as swapping, shifting, ANDing, ORing, and loading to manipulate data and select one of the registers to place the results. If the results are to be stored in memory, for example, the MB Register is loaded and gated onto the MD BUS by MD DIR L. This same information is carried to the inhibit drivers and stored in the selected memory location. If an option such as the EAE that is plugged into the OMNIBUS wanted the results of the data manipulation, the data path is from the MAJOR REGISTERS BUS to the DATA BUS. This condition is caused by loading either the MQ or the AC with the data and enabling the transfer of the data onto the DATA BUS. To place the data contained in some memory location onto the DATA BUS, the memory location must first be selected. The content of the memory location must be sensed and applied to the Memory Register. Signal MD DIR L gates the Memory Register out to the MD BUS. From the MD BUS the data is applied to the Register Multiplexer and to the MAJOR REGISTERS BUS via the adder and output multiplexer. Signal AC → BUS L places the data onto the DATA BUS.

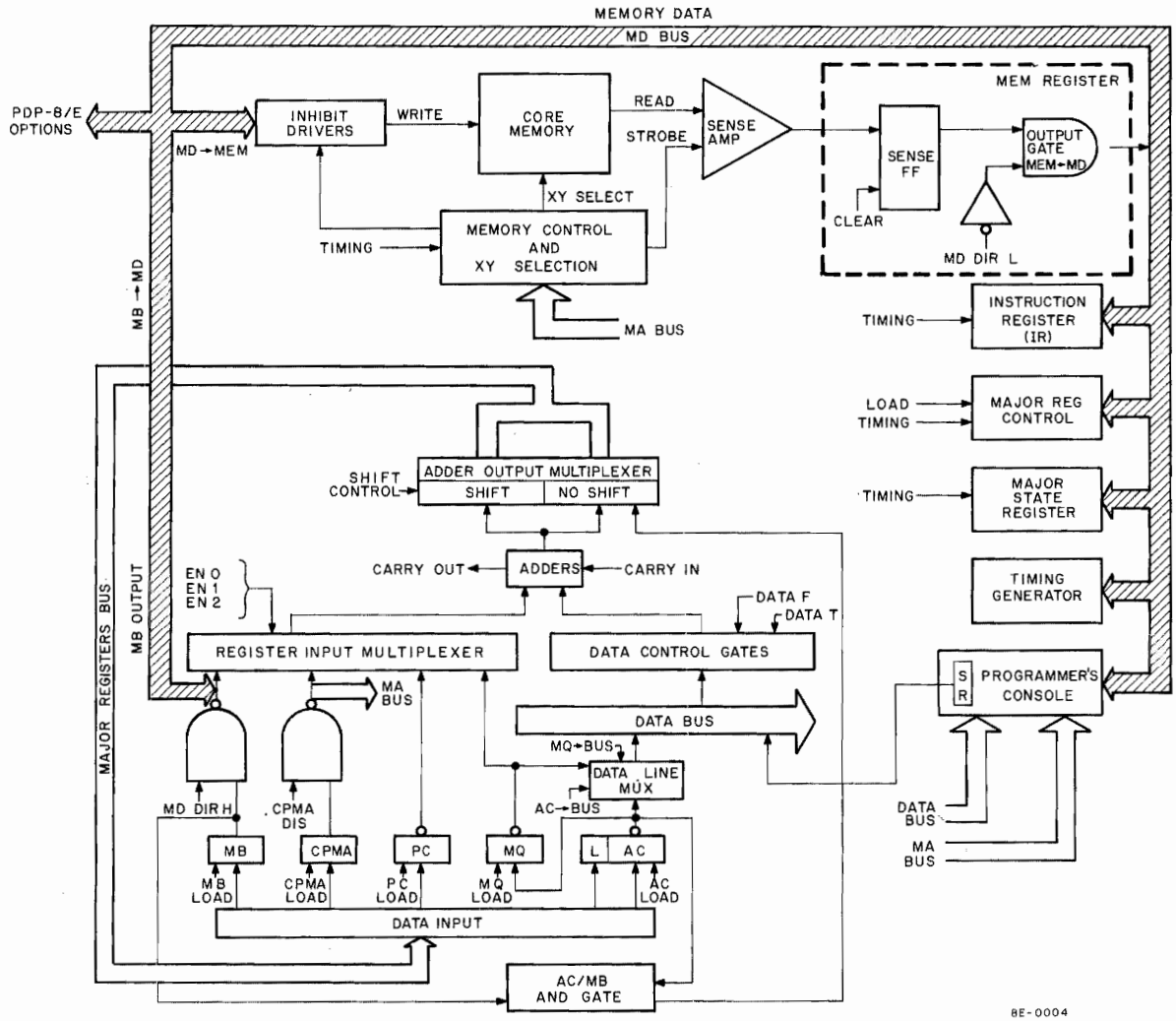

Figure 3-2 Basic Data Paths

3.3.1 Basic Transfer Control Signals

Table 3-2 traces the data paths (Figure 3-2) from the major registers through to the MAJOR REGISTERS BUS and returns to a selected register. Each control signal is referenced to the detailed logic description; thus, the reader can see how the control signal is developed.

Table 3-2
Basic Transfer Control Signals

From	To	Basic Control Signal	Logic Reference
SWITCH Register	DATA BUS	DEPOSIT	3.33.1.1
SWITCH Register	DATA BUS	LOAD ADDRESS	3.33.1.1
AC Register	DATA BUS	AC → BUS	3.35.2
MQ Register	DATA BUS	MQ → BUS	3.35.2
AC Register	MQ REG	AC → MQ ENA LOAD MQ	3.40
DATA BUS	ADDERS	DATA T DATA F	3.35.3
Complement of DATA BUS	ADDERS	DATA T DATA F	3.35.3
MQ Register	ADDERS	EN0 EN1 EN2	3.35.1
PC Register	ADDERS	EN0 EN1 EN2	3.35.1
CPMA Register	ADDERS	EN0 EN1 EN2 CPMA DIS L	3.35.1 asserted low by options
CPMA Register	MA BUS	CPMA DIS L	
MB Register	MD BUS	MD DIR L	3.28
MD BUS	ADDERS	EN0 EN1 EN2	3.35.1
MAJ REG BUS	MB REG	MB LOAD L	3.37.1

Table 3-2 (Cont)
Basic Transfer Control Signals

From	To	Basic Control Signal	Logic Reference
MAJ REG BUS	CPMA REG	CPMA LOAD L	3.37.4
MAJ REG BUS	PC REG	PC LOAD L	3.37.3
MQ MUX	MQ REG	MQ LOAD L	3.40
MAJ REG BUS	AC REG	AC LOAD L	3.37.2
CPMA	CPMA + 1	CARRY IN L	3.36.1
PC	PC + 1	CARRY IN L	3.36.1
MEM REG	MD BUS	MD DIR L	3.28

FROM ADDERS	TO MAJOR REGISTERS BUS	Logic Reference 3.36.2

Type of Operation	Shift Control Signals				
	PAGE Z L	RIGHT L	LEFT L	TWICE L	
ZEROs TO MA 0–4 (PAGE ZERO)	H	L	L	L	
AND MB WITH (MB•AC)	L	L	L	H	
SHIFT OUTPUT OF ADDERS RIGHT ONCE	L	L	H	H	
SHIFT OUTPUT OF ADDERS LEFT ONCE	L	H	L	H	
SHIFT OUTPUT OF ADDERS RIGHT TWICE	L	L	H	L	
SHIFT OUTPUT OF ADDERS LEFT TWICE	L	H	L	L	
BYTE SWAP (SWAP first six bits with last six bits)	L	H	H	L	
NO SHIFT	L	H	H	H	

3.4 PROCESSOR BASIC TIMING

Four time states, TS1 through TS4, are provided by the timing generator to divide the processor cycle into four parts (Figure 3-3). The major states control the flow of events during the execution of programmed instructions.

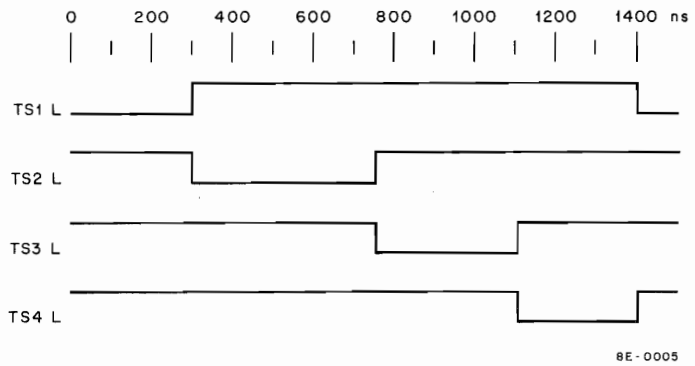

Figure 3-3 Processor Timing States (Slow Cycle)

3.5 PROCESSOR MAJOR STATES FLOW

The PDP-8/e provides four major states:

a. FETCH, to obtain the Memory Reference Instruction and Nonmemory Reference Instructions from memory, and perform Nonmemory Reference Instructions

b. DEFER, for indirect addressing or autoindexing

c. EXECUTE, for performing the Memory Reference Instruction

d. Direct Memory Access (DMA), for manual operation or data break.

The basic major state flow diagram is illustrated in Figure 3-4. This diagram also indicates the order in which the major states are implemented. For any type of processor instruction, the processor must bring the contents of some memory location to the MD BUS. The Instruction Register (IR) decodes the first three bits (0–2). With FETCH major state asserted and the instruction decoded, the Central Processor (CPU) follows a series of steps; these steps are controlled by timing and the logic of the CPU.

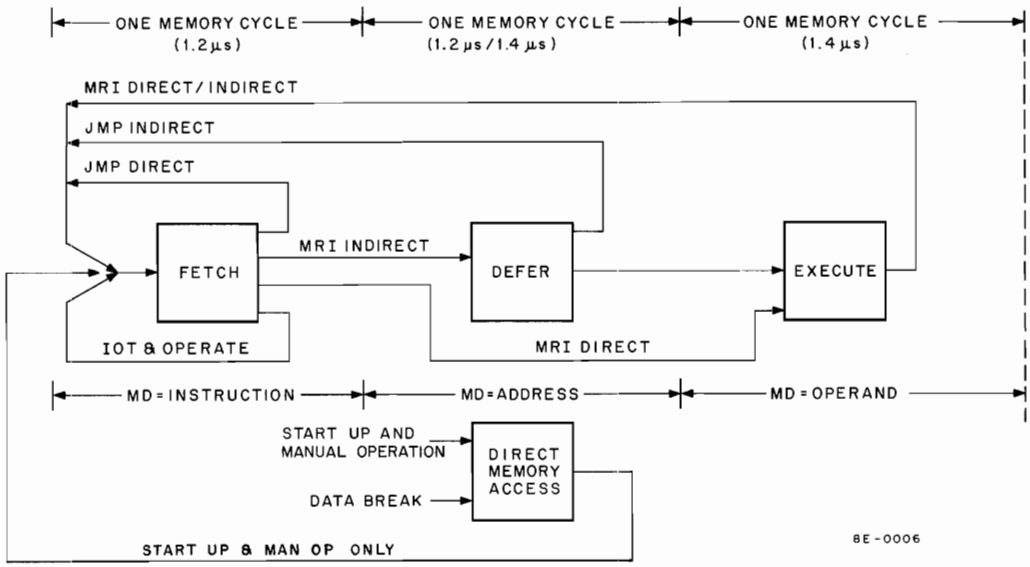

Figure 3-4 PDP-8/E Major State Flow Diagram

The FETCH major state is required for all instructions. For Memory Reference Instructions (MRI), the CPU enters the EXECUTE state via DEFER (for an indirect address) or the EXECUTE state (for a direct address). IOT and OPERATE instructions are completed in one memory cycle during FETCH. However, an MRI can take either 2 or 3 cycles (depending on a direct or indirect address). Most instructions, therefore, take 2.6 μs or 3.8 μs, depending on the addressing.

In Figure 3-4, during the FETCH cycle, the content of the MD BUS is the instruction and an address; during the DEFER cycle, the content of the MD BUS is an address; during the EXECUTE state, the MD BUS contains the operand (that data contained in the addressed location on which the instruction will manipulate or modify). The DEFER cycle is 1.2 μs for an indirect address and 1.4 μs for an autoindex.

A fourth major state is Direct Memory Access (DMA). During the DMA state, manual functions can be accomplished or the data break system can operate. Both the manual and data break operations require access to a memory location with little help from the CPU control.

3.6 START-UP FLOW DIAGRAM

The following information describes the events of the Start-Up flow diagram illustrated in Figure 3-5. A flow reference keys the flow diagram with the corresponding explanation.

Flow Reference	Explanation
(1)	TURN KEY TO POWER – The POWER position of the OFF-POWER-PANEL LOCK switch generates the INITIALIZE signal in the timing generator. INITIALIZE is used to clear the AC Register, the Link, the Skip circuit, flags, etc. Operation of the CLEAR key also generates INITIALIZE.
(2)	LOAD ADDRESS – The operator sets the switch register to the desired address and depresses the ADDR LOAD key. At the same time the address is loaded, signals MS IR DISABLE L and F SET L are asserted; consequently, the next cycle major state is FETCH. If restart is desired, the state of the AC Register, Link circuit, Skip circuit, and flags should be cleared immediately after the address is loaded. CLEAR develops signal INITIALIZE, as previously described.
(3)	EXAMINE OR DEPOSIT – To examine the contents of the addressed memory location or deposit a word into memory, branching into the Dep/Exam Flow (Paragraph 3.8.2) is required. When the operator has finished, the Start-Up flow is resumed.
(4)	DEPRESS CONT KEY – The assertion of the CONT (continue) key asserts MEM START (Paragraph 3.33.1.1) which, in turn, asserts signal RUN (Paragraph 3.16). Because RUN is necessary to start timing, the timing chain begins at the next clock pulse and continues as long as RUN is asserted.
(5)	FETCH CYCLE – The FETCH cycle is automatically entered if D SET L or E SET L of the Major State Register has not been asserted. Refer to Paragraph 3.9 for the FETCH state discussion.

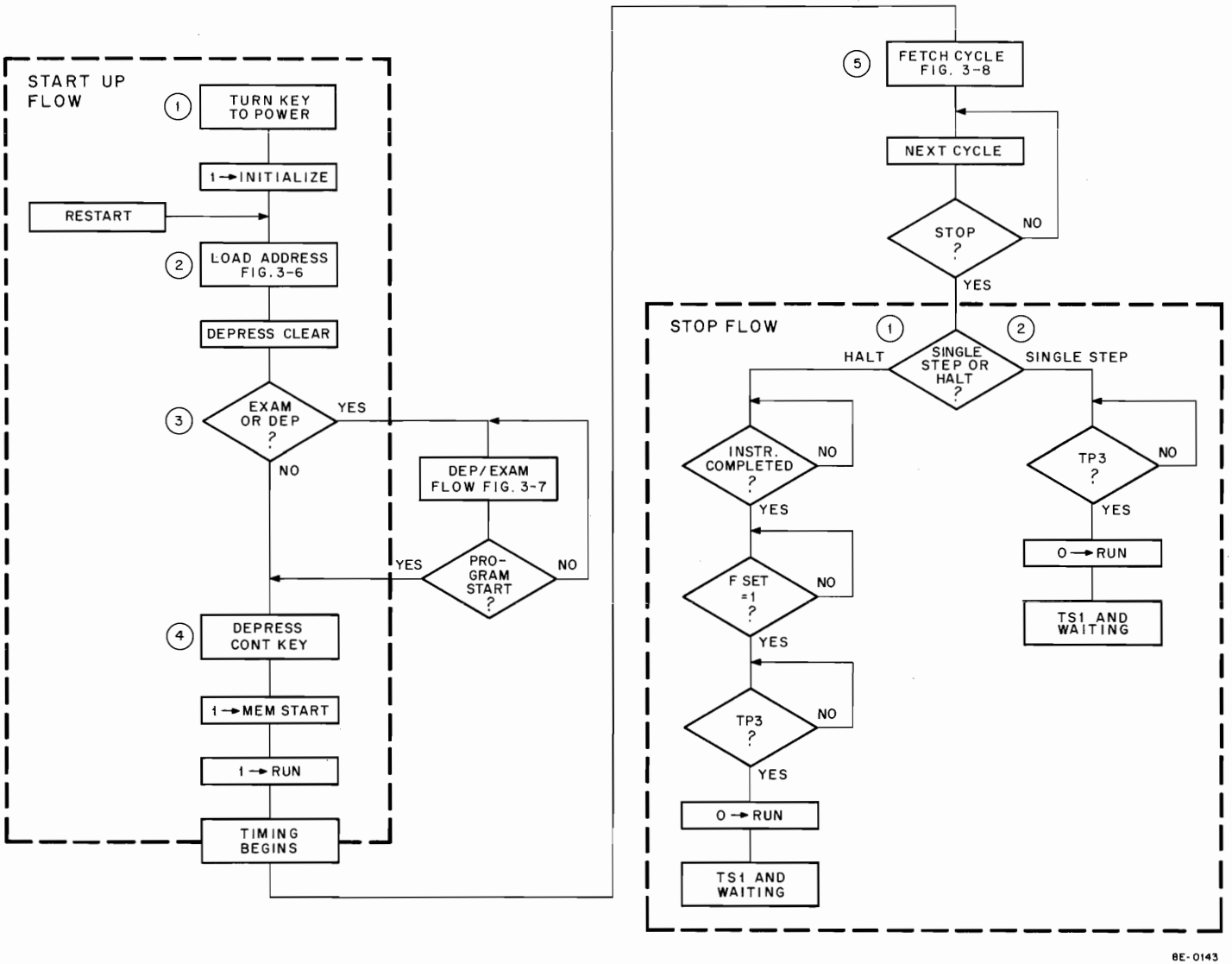

Figure 3-5 Start-Up/Stop Flow Diagram

3.7 STOP FLOW DIAGRAM

The Stop flow diagram is presented in Figure 3-5. The two methods of manually stopping the processor are indicated as either halt or single step.

Flow Reference	Explanation
(1)	HALT – There are two methods of generating a HALT command: (a) program the HALT instruction (Paragraph 3.9.2), or (b) depress the HALT key as shown in Figure 3-5. The HALT command allows the processor to complete the current instruction; this could take up to three processor cycles (FETCH, DEFER, EXECUTE), depending on the type of instruction being processed when the HALT command is received. At TP3 when F SET L is asserted, signal RUN is made inactive (Paragraph 3.16). Thus, the timing chain is interrupted, and the processor is halted in TS1.
(2)	SINGLE STEP – When the SING STEP key is depressed, the processor halts at the end of the current cycle. Because it does not wait until F SET L is asserted, the processor does not necessarily finish the current instruction. (This is the only difference between halt and single step.)

3.8 DIRECT MEMORY ACCESS (DMA) STATE FLOW DIAGRAMS

The Direct Memory Access (DMA) state allows accessing of memory when the Major State Register and Instruction Register of the CPU are disabled. Two types of DMA are available with the PDP-8/E System: (a) the basic type is the use of the Programmer's Console to either deposit into memory or retrieve from memory a 12-bit word, and (b) the second type is called data break and is used with mass storage equipments. A simplified flow diagram representing both types is provided in Figure 3-4. Refer to the *PDP-8/E & PDP-8/M Small Computer Handbook,* Chapter 6, and Volume 3 of this manual for a discussion of data break.

3.8.1 Load Address Flow Diagram

The Programmer's Console is used for manual addressing of memory. Using 12 switches, the operator can load the CPMA Register with a desired address whenever the ADDR LOAD key is depressed. In a similar manner, the Extended Address is loaded. A flow diagram representing the basic functions is presented in Figure 3-6.

Flow Reference	Explanation
(1)	LOAD ADDRESS – A 12-bit address is first set into the switch register, and the ADDR LOAD key is depressed. The following events occur: a. The contents of the Switch Register are transferred onto the DATA BUS. b. The outputs of the Major State (MS) Register and Instruction Register (IR) are disabled; F SET L is asserted. c. The register input multiplexer is disabled. d. The data control gate is enabled. e. Signal CPMA LOAD is asserted, loading CPMA, and setting the FETCH flip-flop in the MS Register.

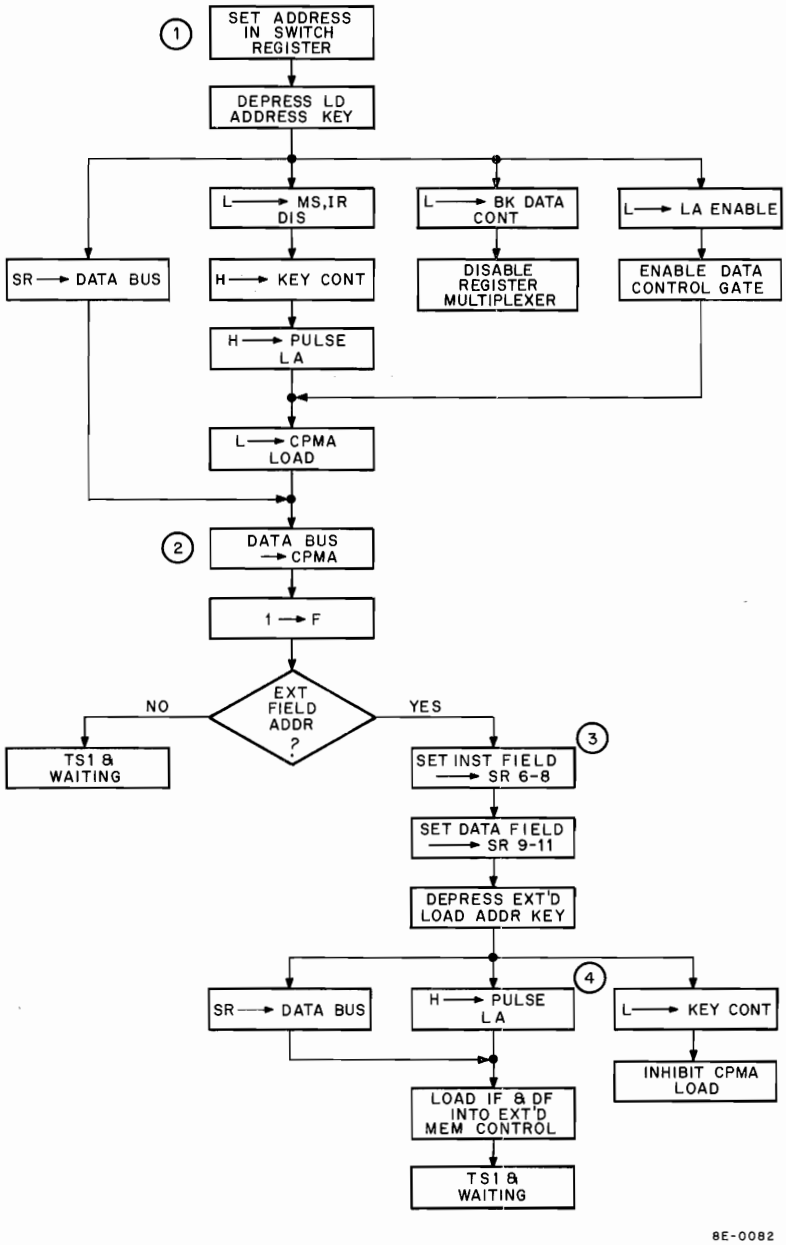

Figure 3-6 Manual ADDR LOAD/EXTD LOAD

Flow Reference	Explanation
(2)	DATA BUS → CPMA – The contents of the DATA BUS (Figure 3-2) follow the path through the data control gate into the adder, through the no shift portion of the output multiplexer, and onto the MAJOR REGISTERS BUS. Signal CPMA LOAD L then gates the contents of the MAJOR REGISTERS BUS into the CPMA Register. FETCH L is developed by CPMA LOAD L (Paragraph 3.34.1). Thus, the processor will be in the FETCH state during the next processor cycle unless direct memory access is again required. However, because the timing chain was never activated during LOAD ADDRESS events, the processor time state will be in TS1 and waiting.
(3)	If extended address is required, the following events must occur: a. Load the Instruction Field into Switch Register (SR) bits 6 through 8. b. Load Data Field into SR bits 9 through 11. c. Depress EXTD ADDR LOAD key.
(4)	The contents of the SR are then transferred to the DATA BUS and applied to the extended memory control module. All circuits within the major registers are inhibited.

3.8.2 Deposit/Examine Flow Diagram

The similarities and differences in the Deposit and Examine events are illustrated in Figure 3-7. For Examine (shown on the left of the figure), it is necessary to read the addressed memory location; for Deposit (shown on the right of the figure), it is necessary to write into the addressed memory location; common events are shown in the center of the figure.

Flow Reference	Explanation
(1)	EXAMINE – Depressing the EXAM key asserts both BRK DATA CONT L and MD DIR L. These signals are necessary to read from memory and also allow the contents of the MD BUS to be applied to the MB Register.
(1)	DEPOSIT – The data word must first be manually selected on the SR. The DEP key is then lifted and the contents of the SR are then applied to the DATA BUS (Figure 3-2).

3.8.2.1 Examine or Deposit Common Events – Depressing either the EXAM or DEP key causes the following events to occur:

Flow Reference	Explanation
(2)	The major states and Instruction Registers are disabled (Paragraph 3.33.1.1).
(3)	Signal RUN L is asserted by MEM START L (Paragraph 3.16) and timing begins.
(4)	Signal STOP is asserted by KEY CONT L. At TP3 time, STOP is used to 0 the RUN flip-flop.

Flow Reference	Explanation
(5)	The contents of the CPMA Register are gated through the Register Input Multiplexer (Figure 3-2) and placed onto the adder circuits. A CAR IN signal is developed (Paragraph 3.36.1), adding 1 to the sum of the adder inputs. The result is then loaded into the PC Register to provide "MA + 1 to the PC".
(6)	MEM TO MD – The READ operation (Paragraph 3.27.2) begins during TS1 and continues into a portion of TS2. This places the contents of the addressed memory location onto the MD BUS (Figure 3-2). Thus, the contents of memory are now ready to be gated onto the MAJOR REGISTERS BUS during TS2.
(7)	EXAMINE – The contents of the MD BUS (12 bits) are gated through the Register Input Multiplexer during TS2 (Paragraph 3.35.1) and placed onto the MAJOR REGISTERS BUS (Figure 3-2). The 12-bit word is now ready to be loaded into the MB Register at TP2. BRK DATA CONT L is pulled low to ENABLE DATA PLUS MD to the MB. The data lines, in this case, are 0s (high).
(8)	DEPOSIT – The contents of the DATA BUS are gated through the Data Control Gate and applied to the MAJOR REGISTERS BUS (Figure 3-2). The 12-bit word is now ready to be loaded into the MB Register.
(8)	MB load occurs at TP2 (Paragraph 3.37.1). At this time, the contents of the MAJOR REGISTERS BUS are loaded into the MB Register.
(9)	With the READ operation completed, it is necessary to write the same information back into memory or deposit new information. However, the contents of the MB Register must first be transferred to the MD BUS. This occurs when MD DIR L is negated (Figure 3-2).
(10)	A 0 is placed in the RUN flip-flop (Paragraph 3.33.1.1) when TP3 and STOP are both asserted. This prevents the processor from starting a new cycle until some action is taken by the operator.
(11)	The WRITE operation automatically starts during TS3 and continues into TS4. At this time, the contents of the MD BUS are written into the addressed memory location.
(12)	For the preparation of the next processor cycle, the next sequential address is automatically placed in the CPMA Register. Because the Program Counter (PC) contains the next address, the contents of the PC are loaded into the CPMA at TP4. If the operator desires to go into programmed operation, the CONT key must be depressed. Because the next active state will be either DMA or FETCH, depressing the EXAM key or raising the DEP key inhibits the Major State Register and allows one more DMA cycle. Otherwise, depressing the CONT key (Figure 3-6) causes a FETCH cycle.
(13)	During TS1 and when RUN = 0, the processor timing stops and waits for the next command from the operator. The contents of the MD BUS can be observed at this time. Also note that the CPMA shows the address for the next cycle and not the address from which the data was examined.

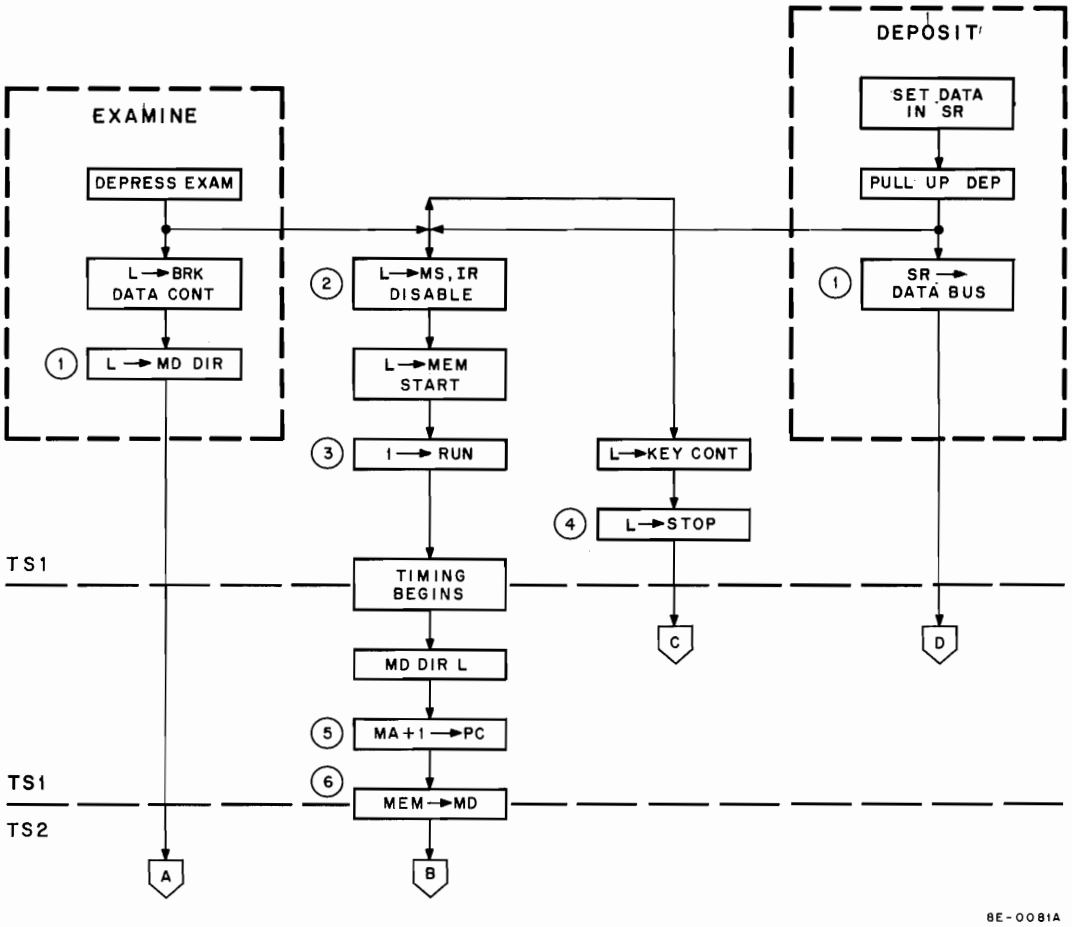

Figure 3-7 Deposit/Examine Flow Diagram (Sheet 1 of 2)

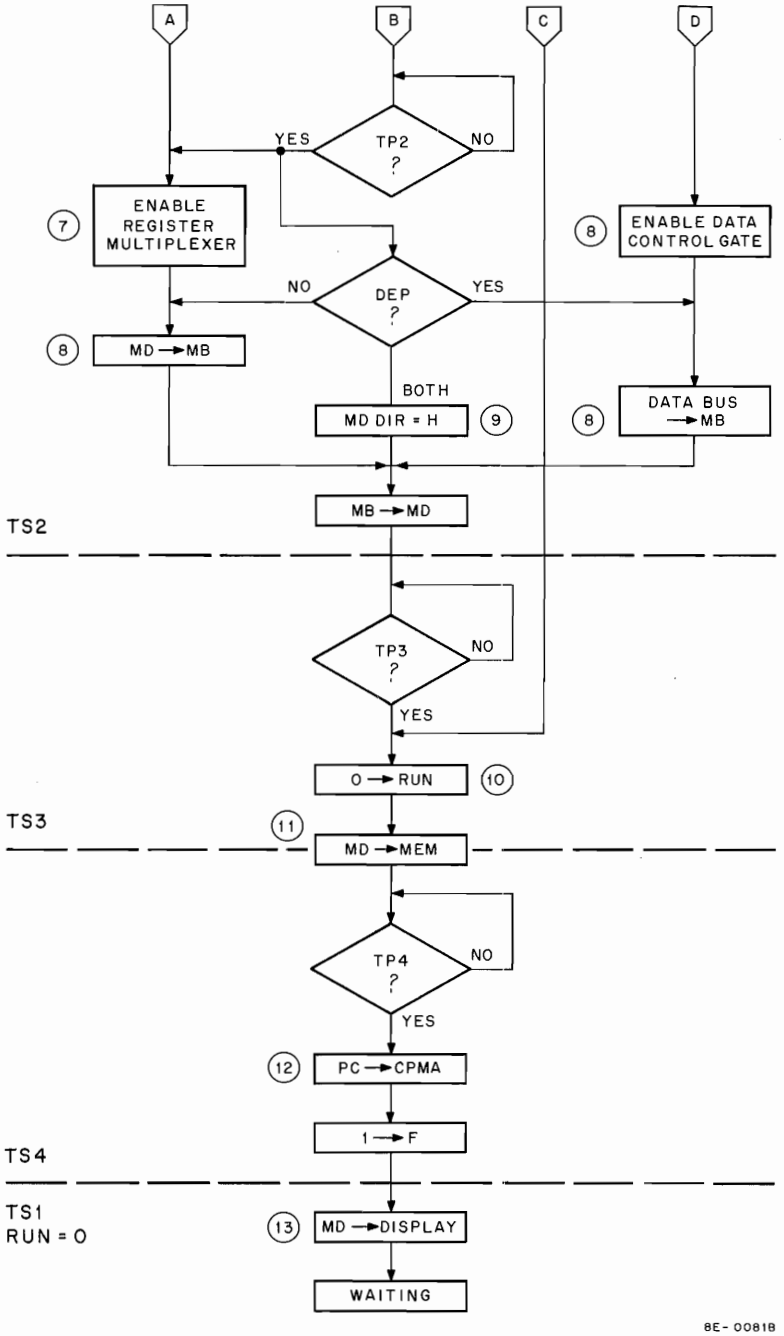

Figure 3-7 Deposit/Examine Flow Diagram (Sheet 2 of 2)

3.9 FETCH STATE INSTRUCTION FLOW DIAGRAM

The logic and instruction flow of events during FETCH is illustrated in Figure 3-8. Because of the complexity of the flow diagrams, the discussion is further divided into subflows as illustrated.

3.9.1 Common Events During FETCH (refer to Figure 3-2 for data paths)

Time State	Common Event
TS1	Update the PC Register, read the addressed memory location, and display the content of Major Registers.
TS2	Read the addressed memory location, transfer the content to the MD BUS, and decode the instruction.
TS3	Perform an augmented instruction (IOT or OPERATE), and begin writing the content of the MD BUS back into the addressed memory location or carry the Memory Reference Instruction to either the DEFER or EXECUTE state. Load the AC Register.
TS4	Update or modify the CPMA and complete the write operation. Enable the next processor major state (FETCH, DEFER, or EXECUTE).

Flow Reference	Explanation
(1)	CLEAR SKIP LOGIC – The SKIP flip-flop (Paragraph 3.38) is cleared during TS1.
(2)	INCREMENT PC – The Carry In logic (Paragraph 3.36.1) is asserted and applied to the adder circuit (bit 11). MA is then brought to the adder circuits and the results placed in the PC.
(3)	TRANSFER AC → PERIPHERAL – The content of the AC is placed on the DATA BUS to be used as determined by the user.
(4)	The content of the Memory Register is gated onto the MD BUS when MD DIR is low.
(5)	During FETCH, the first three bits of MD are decoded by the Instruction Register (Paragraph 3.34.2) to determine the type of instruction to be performed.
(6)	When MD bits 0–2 contain 1s, a 7 is decoded, indicating that an operate instruction is to be performed.
(6)	Three groups of operate instructions are available. The group selected depends on the state of MD3 and MD11. Refer to the following paragraphs for the flow diagrams: Group 1 Paragraph 3.9.2 Group 2 Paragraph 3.9.3 Group 3 Paragraph 3.9.4

Flow Reference	Explanation
(7)	Update CPMA – Before the CPMA can be updated, the interrupt system must be considered. If the INT IN PROG signal is asserted, a JMS is forced into the IR, the major state becomes EXECUTE, and 0s are placed into the CPMA. If the INT IN PROG signal is not asserted, the SKIP L signal is tested next. SKIP L may have been asserted as the result of one of the operate instructions or one of the IOT instructions during TS3. When SKIP L is asserted, a CAR IN L signal is generated which places a 1 in adder stage 11. The Register Input Multiplexer is enabled to allow the content of the PC Register (Figure 3-2) to be applied to the adders. The result is then transferred through the Adder Output Multiplexer to the MAJOR REGISTERS BUS and loaded into the CPMA at TP4. Without SKIP L, only the content of the PC will be loaded into the CPMA. The next major state will be FETCH if an IOT, OPERATE, or direct JUMP is performed. Signal F SET L enables the FETCH state.
(8)	IOT INSTRUCTIONS – When bits MD0 and 1 contain 1s and bit 2 is a 0, a 6 is decoded indicating that an IOT instruction is to be performed. Two types of programmed IOTs are available in the PDP-8/E System. Refer to the following paragraphs for the flow diagrams; I/O Transfers (IOTs) — Paragraph 3.9.5 Programmed Interrupt System — Paragraph 3.9.6
(9)	JUMP Instruction – When the decoded instruction is 5_8, the PC is modified during TS3. If MD3 L = 0, the new PC is transferred to the CPMA, and the next cycle is FETCH. If MD3 L = 1, the CPMA is modified in the same manner as the PC, and the next cycle is DEFER. Refer to Paragraph 3.9.7 for the flow diagram and an explanation of the JUMP instruction.
(10)	When instructions AND, TAD, ISZ, DCA, and JMS are decoded during FETCH, the processor examines the page bit (MD4 L) and the direct/indirect address bit (MD3 L) to determine if the next address is on Page 0 or the current page, and if the next address contains an address or data. The result is the entrance into the DEFER state or the EXECUTE state. No other operation is performed with these instructions during FETCH.
(11)	Modify CPMA – The page bit is first examined to determine if the next address is on the current page (MD4 L = 1) or Page 0 (MD4 L = 0). When MD4 L = 0, signal PAGE Z is asserted. This places 0s onto the first five stages of the Adder Output Multiplexer. The last seven bits of the MD BUS are applied directly to the Adder Output Multiplexer. All 12 bits are applied to the MAJOR REGISTERS BUS and loaded into the CPMA at TP4. If PAGE Z L is not asserted, MA0 L – MA4 L are applied to the output of the Adder Output Multiplexer. Bit 3 is then examined; if bit 3 = 1, signal D SET L is asserted and the next cycle is DEFER. Otherwise, E SET L is asserted, and the processor obtains data rather than a new address.

NOTE

Refer to Jump Instruction (Paragraph 3.9.7) and the memory addressing discussion in Chapter 4 of the PDP-8/E & PDP-8/M Small Computer Handbook.

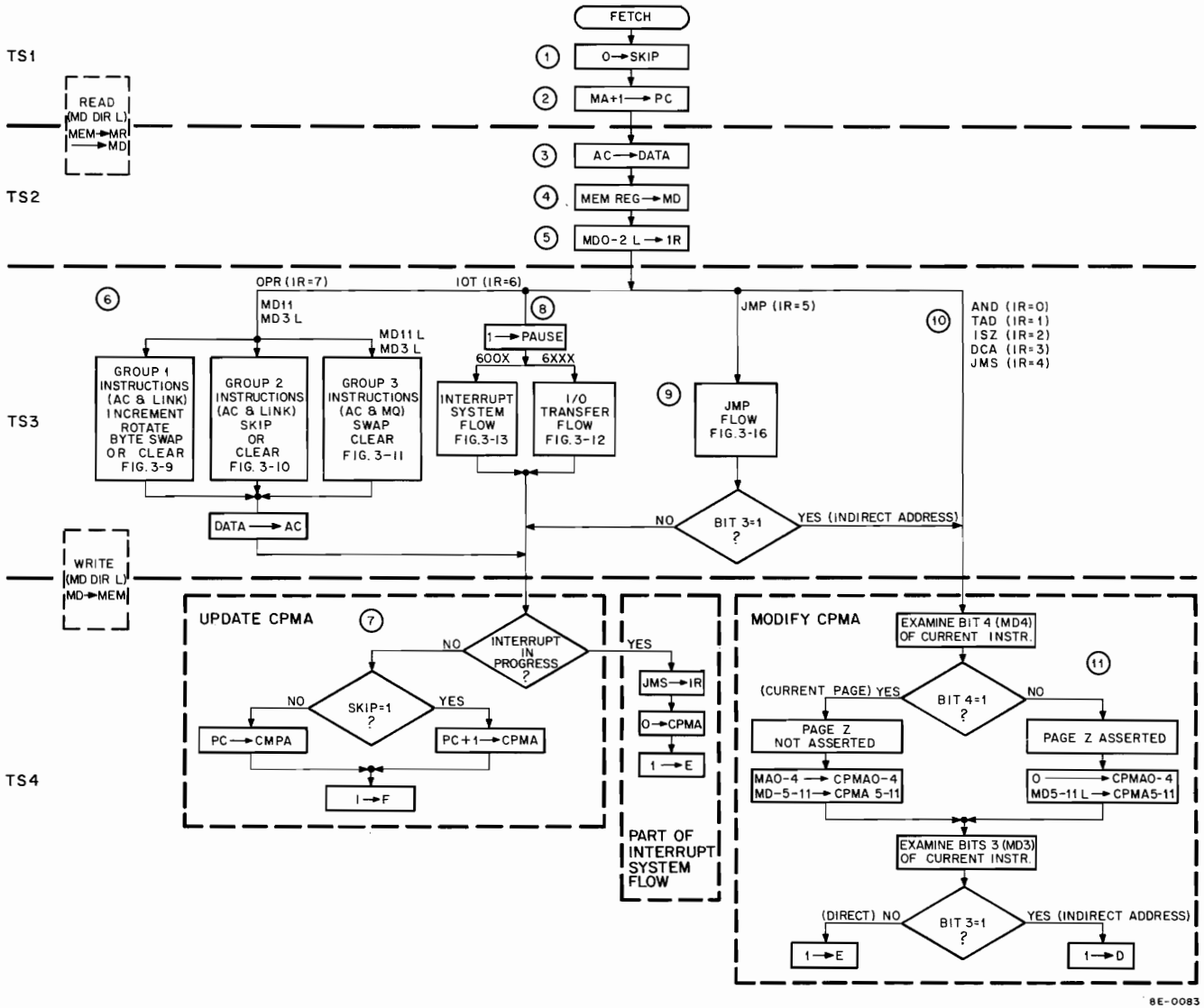

Figure 3-8 FETCH State Flow Diagram

3.9.2 Group 1 Operate Microinstructions Flow Diagram

Group 1 operate microinstructions are established when IR = 7 and when MD3 L = 0 is decoded. Eleven basic instructions are illustrated in Figure 3-9.

3.9.2.1 Data Paths – The data path for all Group 1 instructions is illustrated in Figure 3-2. The common gating and control signals are listed below:

Data Path	Control Signal		Source
AC to DATA BUS (exception is 7200)	AC → BUS L		Paragraph 3.35.3
DATA BUS to adders	True:	DATA T DATA F	Paragraph 3.35.3
	Complement:	DATA T DATA F	DATA T
Adder Output Multiplexer to MAJOR REGISTERS BUS	PAGE Z always L RIGHT L LEFT L TWICE L or none of these		Paragraph 3.36.2
LINK-ADDER-OUTPUT MUX to LINK	LINK data and clock		Paragraph 3.39
MAJOR REGISTERS BUS to AC Register	AC LOAD L		Paragraph 3.37.2

3.9.2.2 Basic Instructions

7000 – NOP – The NOP instruction allows the processor to cycle through one memory cycle with no important operation being implemented during TS3. Note that an AC-to-AC and LINK-to-LINK transfer is accomplished.

7001 – Increment AC – The content of the AC Register is applied to the DATA BUS when AC → BUS L is asserted. DATA F is high and DATA T L is low to allow the content of the bus to be applied to the adders. MD11 L forces a 1 into the adders from the carry in logic. The 1 is applied to bit 11 of the adders; the result is applied to the data input of the AC Register. AC and LINK are loaded during TP3.

7002 – BYTE SWAP – The first six bits of the AC Register are swapped with the last six bits. The content of the AC Register is placed on the DATA BUS and then applied to the adders by DATA T L and DATA F. AC → DATA BUS is enabled by MD4 L and MD7 L = 0. Signal TWICE L is asserted when MD10 L = 1 and will cause a parallel shift right six positions when MD8 L and MD9 L = 0. AC and LINK are loaded during TP3. However, LINK is unchanged.

7004 – Rotate Once Left – The contents of the AC are placed on the DATA BUS by signal AC → BUS L. DATA F and DATA T L apply the DATA BUS to the adders. MD9 L enables the shift left logic, and the asserted signal (LEFT) is applied to the Adder Output Multiplexer. AC and LINK are loaded during TP3.

7006 – Rotate Twice Left – The content of the AC is placed on the DATA BUS. DATA F and DATA T L apply the DATA BUS to the adders. MD9 L asserts the shift left logic signal and MD10 L asserts the TWICE signal; this moves the outputs of the adders two places to the left. The outputs at the output multiplexers are then loaded into the AC Registers and LINK at TP3.

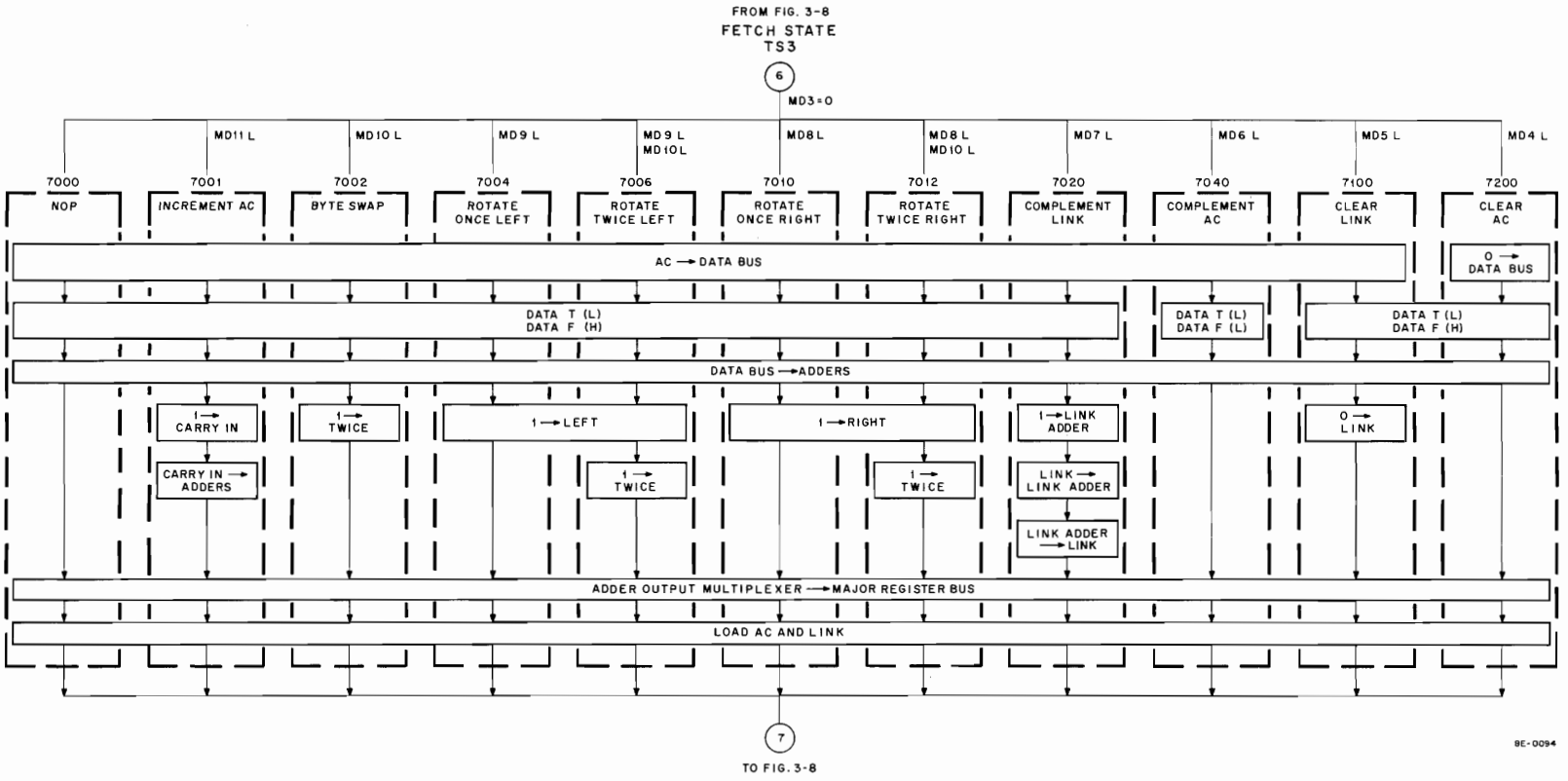

Figure 3-9 GROUP 1 Operate Microinstructions (1 Cycle)

7010 – Rotate Once Right – The content of the AC is placed on the DATA BUS. DATA F and DATA T L apply the DATA BUS to the adders. MD8 L develops signal RIGHT L of the shift right logic. Signal RIGHT L is applied to the output multiplexer circuit, which shifts the contents of the output multiplexers one place to the right. The outputs are then loaded into the AC Registers and LINK at TP3.

7012 – Rotate Twice Right – The content of the AC is placed on the DATA BUS. DATA F and DATA T L apply the DATA BUS to the adders. MD8 L develops signal RIGHT L and MD10 L develops TWICE L. When these two signals are applied to the Adder Output Multiplexer, the contents of the adders are shifted two places to the right. The result is loaded into the AC and LINK at TP3.

7020 – Complement LINK – MD7 L forces a 1 into the LINK circuit. The result will force a 1 to a 0 or a 0 to a 1.

7040 – Complement AC Register – The signal AC → DATA BUS L is first generated; DATA T L and DATA F are asserted so that if 1 is on the DATA BUS, a 0 is placed into the adder or if a 0 is on the DATA BUS, a 1 is placed into the adder. The AC Register is loaded at TP3.

7100 – Clear LINK – A 0 is forced into the LINK circuit when MD5 L = 1, during OPR 1.

7200 – Clear AC – DATA T L is low, DATA F is high. MD4 L disqualifies AC → BUS Logic. This causes 0s to be gated onto the DATA BUS. The contents of the DATA BUS are gated through the Data Control gate and applied to the adders and loaded into the AC Register at TP3 time.

3.9.2.3 Combining Group 1 Microinstructions – Because each instruction takes one memory cycle, it may be desirable to combine many of the instructions so that two instructions can be implemented in one memory cycle. For example, instruction 7001 can be combined with instruction 7040 to give 7041. This combines flow 7001 with flow 7040. The resulting instruction will now complement and increment the AC Register. If a 1 is to be placed into the LINK, instructions 7100 and 7020 can be combined to give 7120. The combined instruction list for commonly used Group 1 operate instructions is as follows:

7041	CIA	Complement and increment AC
7120	STL	Set LINK to a logical 1
7204	GLK	Get LINK and place content into AC bit 11
7300	CLA CLL	Clear AC and LINK
7240	CLA CMA	Set AC = - 1
7201	CLA IAC	Set AC = 1
7110	CLL RAR	Shift positive 1 right
7104	CLL RAL	Shift positive 1 left
7106	CLL RTL	Clear LINK, rotate 2 left
7112	CLL RTR	Clear LINK, rotate 2 right

3.9.3 Group 2 Operate Microinstructions Flow Diagram

Group 2 operate microinstructions are established when MD3 L (1) and MD11 (L) 0 are decoded. Ten basic instructions are provided in Group 2 (Figure 3-10).

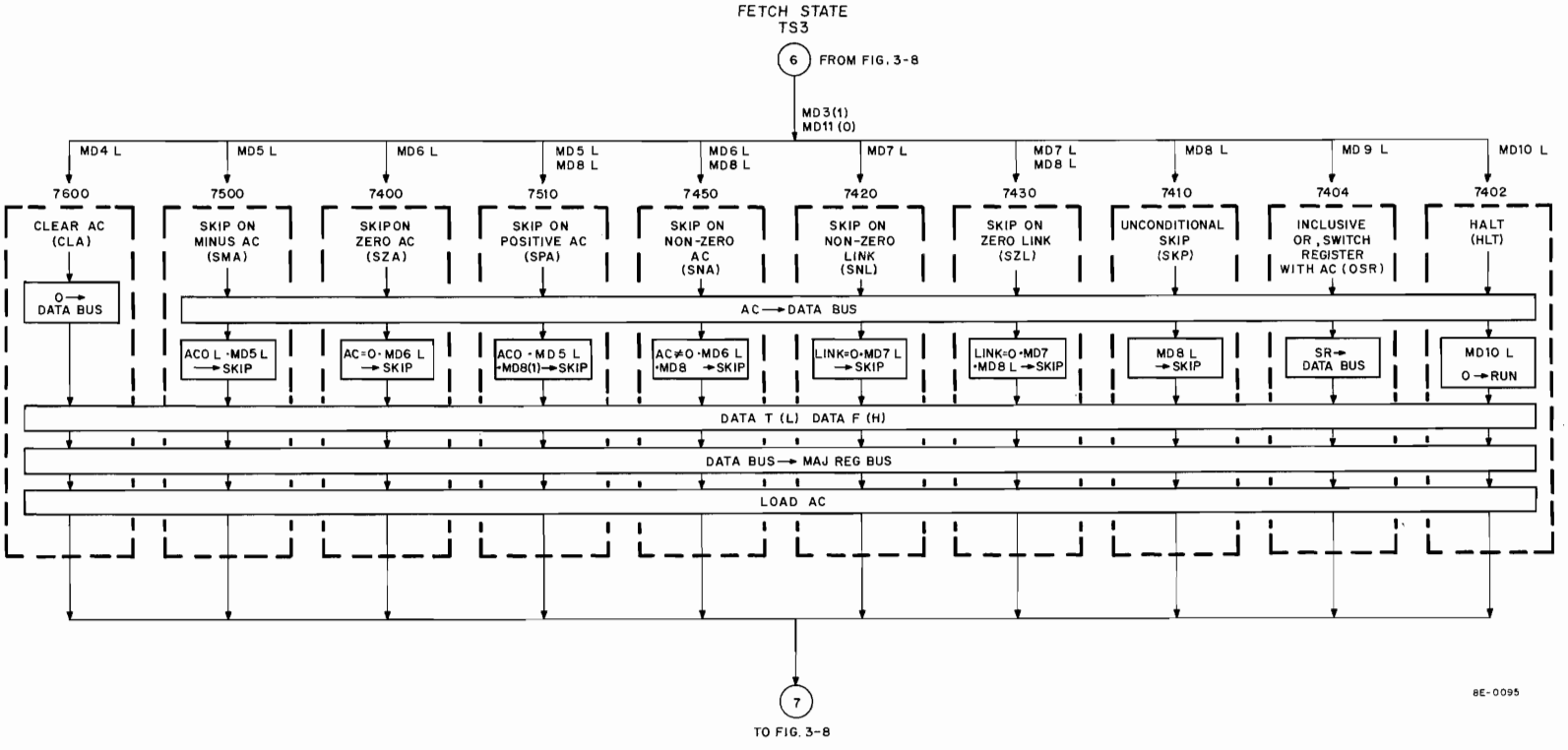

Figure 3-10 GROUP 2 Operate Microinstructions (1 Cycle)

3.9.3.1 Data Path – The data path for all Group 2 instructions is illustrated in Figure 3-2. The common gating and control signals are listed below:

Data Path	Control Signal	Source
AC to DATA BUS (the exception is 7600)	AC → BUS L	Paragraph 3.35.2
DATA BUS to Adders	DATA T DATA F	Paragraph 3.35.3
Adders to Adder Output Multiplexer	None	
Adder Output Multiplexer to MAJOR REGISTERS BUS	None	
MAJOR REGISTERS BUS to AC Register	AC LOAD L	Paragraph 3.37.2

3.9.3.2 Basic Group 2 Instructions

7600 – Clear AC (CLA) – Signal AC → BUS L is not asserted causing a 0 to be gated into the adder circuits. At TP3 time, 0s are loaded into the AC.

7500 – Skip on Minus AC (SMA) – The skip logic tests AC0 for a 1 when MD5 L = 1, indicating that the AC contains a negative 2's complement number. A 1 is then placed in the SKIP flip-flop. During TS4, the content of the PC is incremented by 1 so that the next sequential instruction is skipped.

7440 – Skip on Zero AC (SZA) – The skip logic tests the accumulator for all 0s when MD6 L is asserted with MD8 L (0). If AC = 0, the SKIP flip-flop is set.

7510 – Skip on Positive AC (SPA) – The skip logic tests AC0 for a 0 when MD5 L (1) and MD8 L (1) are asserted. If AC0 = 0, the SKIP flip-flop is set.

7450 – Skip on Non-Zero AC (SNA) – The skip logic tests the contents of the AC Register for all 0s. If one or more AC bits equal 0, a Skip signal is developed when MD6 L and MD8 L are asserted.

7420 – Skip on Non-Zero LINK (SNL) – The skip logic tests the LINK for 1. If LINK = 1, MD7 L = 1, and MD8 L = 0, the SKIP flip-flop will be set.

7430 – Skip on Zero LINK (SZL) – The skip logic tests the link for a 0. When LINK = 0, MD7 L = 1 and MD8 L = 1, the SKIP flip-flop is set.

7410 – Unconditional Skip (SKP) – When MD5 L – MD7 L = 0 and MD8 L = 1, the skip logic sets the SKIP flip-flop.

7404 – Inclusive OR – Switch Register with AC – (OSR) – The contents of the AC Register are transferred to the DATA BUS with signal AC →BUS L asserted. The content of the Switch Register is gated to the DATA BUS when MD9 L = 1 during a Group 2 operate instruction. Signals DATA F and DATA T L gate the ORed content of the DATA BUS through the adders and Output Multiplexers to the input of the AC Register. The AC is loaded during TP3 time. The Link circuit is not affected.

7402 – HALT (HLT) – MD10 L is used to generate a signal (STOP L) that clears the RUN flip-flop, located on the timing generator module. At the next TS1, the processor stops.

3.9.3.3 Combining Group 2 Microinstructions – Combinations of the 10 instructions are listed below:

7604	LAS	Clear AC, and load AC with Switch Register
7640	SZA CLA	Skip if AC = 0, then clear AC
7460	SZA SNL	Skip if AC = 0, or LINK is 1, or both
7650	SNA CLA	Skip if AC $\neq$ 0, then clear AC
7700	SMA CLA	Skip if AC is $<$ 0, then clear AC
7540	SMA SZA	Skip if AC $\leqslant$ 0
7520	SMA SNL	Skip if AC $<$ 0 or LINK = 1, or both
7530	SPA SZL	Skip if AC $\geqslant$ 0, and if LINK is 0
7550	SPA SNA	Skip if AC $>$ 0
7710	SPA CLA	Skip if AC $\geqslant$ 0, then clear AC
7470	SNA SZL	Skip if AC $\neq$ 0, and LINK = 0

NOTE

If Skip instructions are combined and MD8 L = 1, the Skip occurs only if all conditions are simultaneously met. (SPA, SNA, SZL are ANDed.)

If Skip instructions are combined and MD8 L = 0, the Skip occurs if any condition is met. (SMA, SZA, SNL are ORed.)

3.9.4 Group 3 Operate Microinstructions

Group 3 operate microinstructions are established when MD3 L (1) and MD11 L (1) are decoded. Eight Group 3 operate microinstructions are illustrated in Figure 3-11. Six instructions involve operations between the AC and MQ Registers.

3.9.4.1 Data Paths – The data path for all Group 3 operate instructions is illustrated in Figure 3-2. The common gating and control signals are listed below:

Data Path	Control Signal	Source
MQ to DATA BUS	MQ → BUS L	Paragraph 3.35.2
AC to DATA BUS	AC → BUS L	Paragraph 3.35.2
AC to MQ	AC → MQ EN L MQ LOAD L	Paragraph 3.40
DATA BUS to Adders	DATA T L DATA F	Paragraph 3.35.3
Adder Output Multiplexer to MAJOR REGISTERS BUS	None	
MAJOR REGISTERS BUS to AC Register	AC LOAD L	Paragraph 3.37.2
MQ MUX to MQ Register	MQ LOAD L	Paragraph 3.40

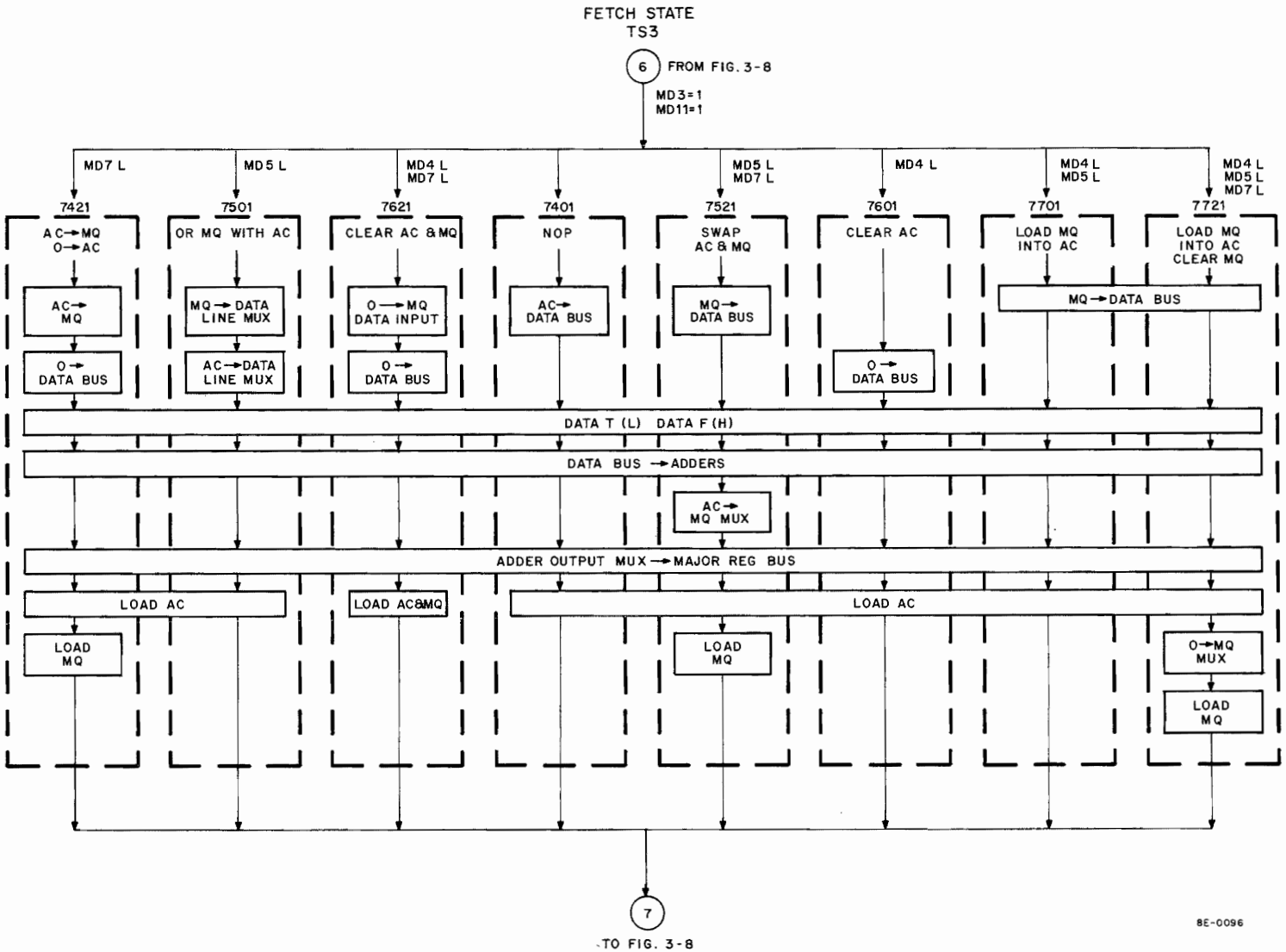

Figure 3-11 Group 3 Operate Microinstructions (1 Cycle)

3.9.4.2 Basic Group 3 Instructions

7421 – Load MQ from AC and Clear AC Register – The content of the AC Register is gated to the data inputs of the MQ Register by the MQ MUX. MQ is loaded by TP3, MD3 L – MD7 L, and MD11 L to clear the AC Register. AC → BUS L is not asserted; this places 0s on the DATA BUS. The 0s follow the data path through the Data Control Gate, through the adders, and are loaded into the AC Register at TP3.

7501 – OR MQ with AC – The contents of the MQ and AC Registers are transferred to the MAJOR REGISTERS BUS during TS3. ORing is accomplished in the Data Line MUX on a bit-by-bit basis. The result is applied to the adder and subsequently applied to the data input of the AC Register. At TP3, the AC Register is loaded.

7621 – Clear AC and MQ – Signal AC → BUS L is not asserted so that only 0s are applied to the adder circuits. AC → MQ EN L is high (MD4 L = 1), disabling the MQ MUX and, thus, placing 0s at the input to the MQ. The AC and MQ are both loaded at TP3.

7401 – NOP – No instructions are executed during NOP. The AC Register is loaded at TP3. The AC is on the DATA BUS and DATA T L is grounded.

7521 – SWAP AC and MQ – The outputs of the AC and MQ Registers take separate paths to accomplish a swap. The MQ Register output is allowed to go through the adders as a result of the MQ → BUS L control signal. The output of the AC Register is applied to the MQ MUX and gated into the MQ Register at TP3. The AC Register is also loaded at TP3.

7601 – Clear AC Register – Signal AC → BUS L is not asserted. Thus, 0s are passed through the adders and applied to the data inputs of the AC Register. At TP3 time, the AC Register is loaded.

7701 – Load MQ Register into AC Register – The contents of the MQ Register are brought into the Data Bus MUX and gated onto the Data Control Gate by MQ → BUS L enabling signal. Data enabling signals DATA T L and DATA F gate the data out to the adders and to the MAJOR REGISTERS DATA BUS. This places the data at the data input of the AC Registers. During TP3, the data is loaded into the AC Register.

7721 – Load MQ into AC and Clear MQ – The contents of the MQ Register are gated through the Data LINE MUX (Paragraph 3.34) to the Data Bus by signal MQ → BUS L. DATA T and DATA F, gate the contents to the adders and, hence, to the data input of the AC Registers. AC → MQ EN L is high, placing 0s at the input to the MQ Registers. The AC and MQ are loaded at TP3.

3.9.5 I/O Transfer Flow Diagram

The I/O transfer flow diagram is presented in Figure 3-12. There are seven sets of conditions to cause I/O transfers and six types of data transfers:

a. Data may be received from a device, ORed with the AC, and the result placed into the AC.
b. Data may be received from a device to be added to contents of the PC.
c. Data may be received from a device to replace the contents of the PC.
d. Data may be sent to a device, and the AC Register cleared.
e. Data may be received from a device and loaded into the AC.
f. Data may be sent to a device.

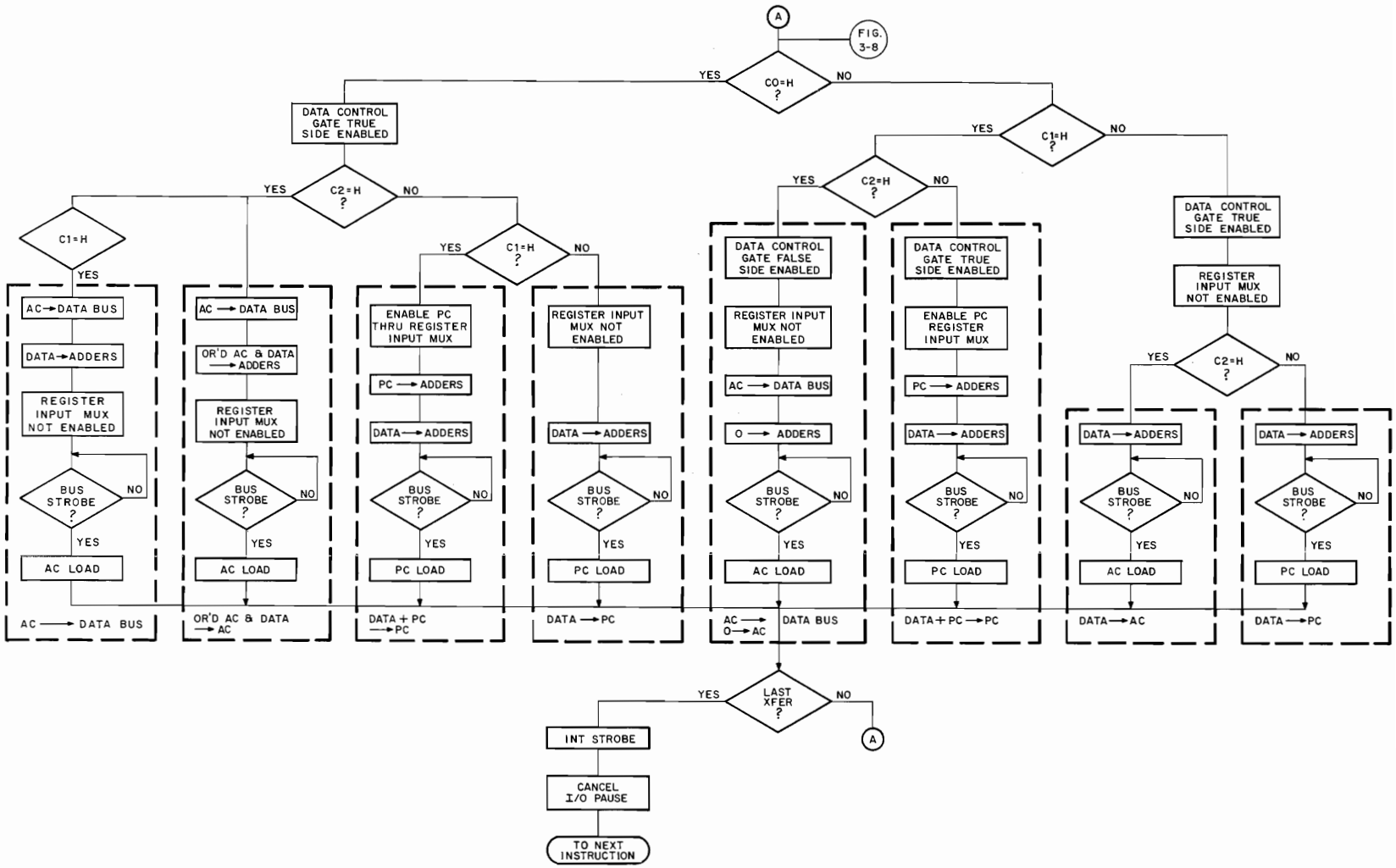

Figure 3-12 I/O Transfer Flow Diagram

The primary control signals for I/O transfer, C0 L, C1 L, C2 L, are generated by the device control logic. These signals are used to indirectly control the Register Input Multiplexer and the data control gate (Figure 3-2) through development of enabling signals EN0 L, EN1 L, EN2 L, for the Input Multiplexer and DATA T L/DATA F signals for the data control gate.

Any device control logic that is connected to the positive I/O bus interface module or requires longer than 1.2 μs provides an additional control signal called NOT LAST TRANSFER L. When this signal is asserted, the timing of the processor stops during TS3 and does not start again until the NOT LAST TRANSFER L signal is no longer asserted and BUS STROBE L is generated. At this time, INT STROBE is asserted, and I/O PAUSE L is negated. If the I/O is high-speed and internal (not involving the positive I/O bus interface), both I/O PAUSE L and INTERNAL I/O L are negated.

3.9.6 Programmed Interrupt System Flow Diagrams

The programmed interrupt system flow diagram is illustrated in Figure 3-13. The basic interrupt system includes:

a. If interrupted, complete instruction and JMS to location 0.

b. Store return address and turn off interrupt.

The interrupt service program handles the determining of the interrupting device, clearing of the flag causing the interrupt, and restoring of the processor to its original condition.

The flow diagram (Figure 3-13) assumes that the interrupt system was turned on during the restoration housekeeping routine.

Flow Reference	Explanation
(1)	CHECK INTERRUPT REQUEST LINE – During the next processor cycle, after the interrupt system was turned on (with instruction ION), the INT DELAY flip-flop is set at TP1 (Paragraph 3.42). This is a necessary condition to set the INT SYNC flip-flop. Because any instruction begins during FETCH and may take several cycles before completion, the last instruction cycle asserts F SET L. At this time, the Interrupt Request line may be tested. If there is no Interrupt Request, the processor returns to the beginning of the FETCH state for the next instruction. Otherwise, it will begin servicing the interrupt.
(2)	With the Interrupt Request line asserted, and the INT DELAY flip-flop set, the INT SYNC flip-flop is set. This asserts the INT IN PROG line which, in turn, forces a JMS into the IR and asserts F E SET. Thus, on the next processor cycle, the EXECUTE major state will be active to store the return address. Because the Register Input Multiplexer (Figure 3-2) is not enabled to allow the PC to transfer to the CPMA during TS4, 0 will be loaded into the CPMA at TP4.
(3)	TURN OFF INTERRUPT SYSTEM – During the EXECUTE major state, the Interrupt System is turned off by clearing the interrupt enable (INT EN) flip-flop, which clears the INT DELAY and INT SYNC flip-flops, negating INT IN PROG.

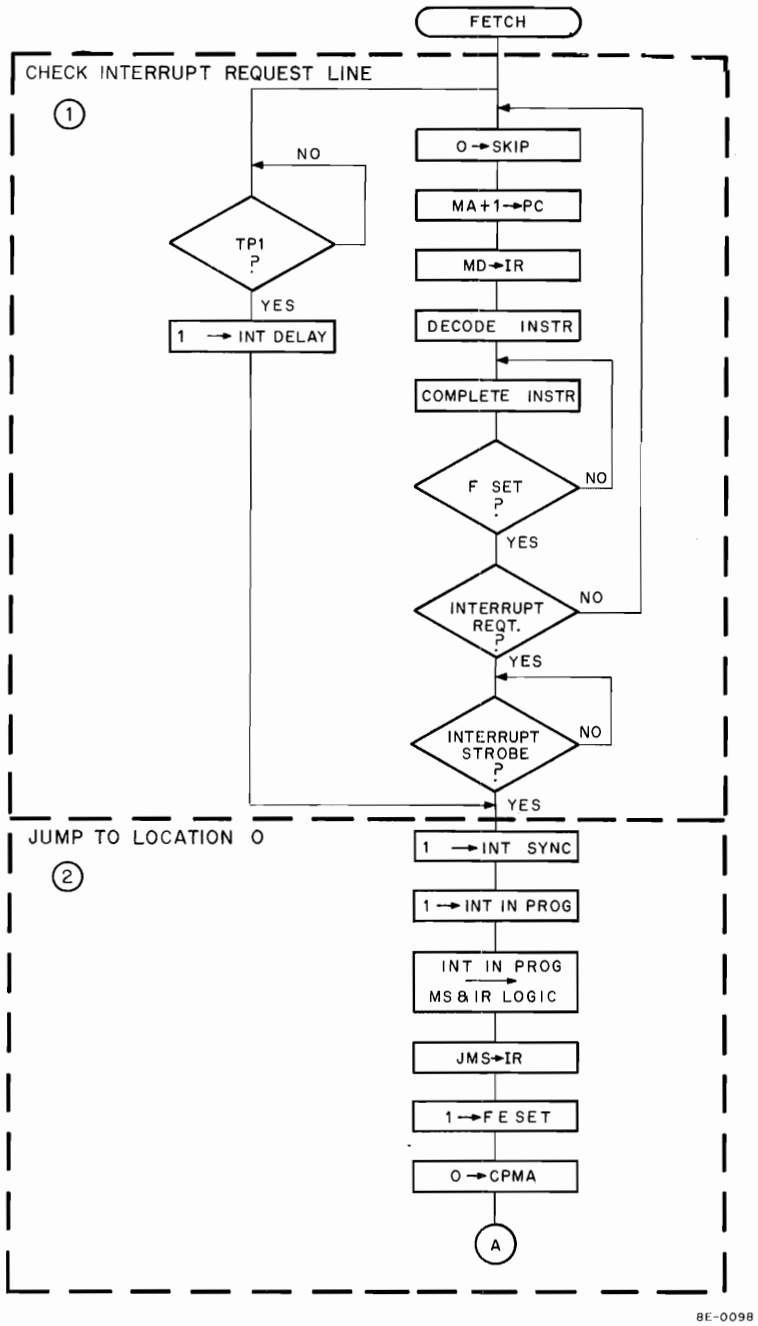

Figure 3-13 Programmed Interrupt System Flow Diagram (Sheet 1 of 2)

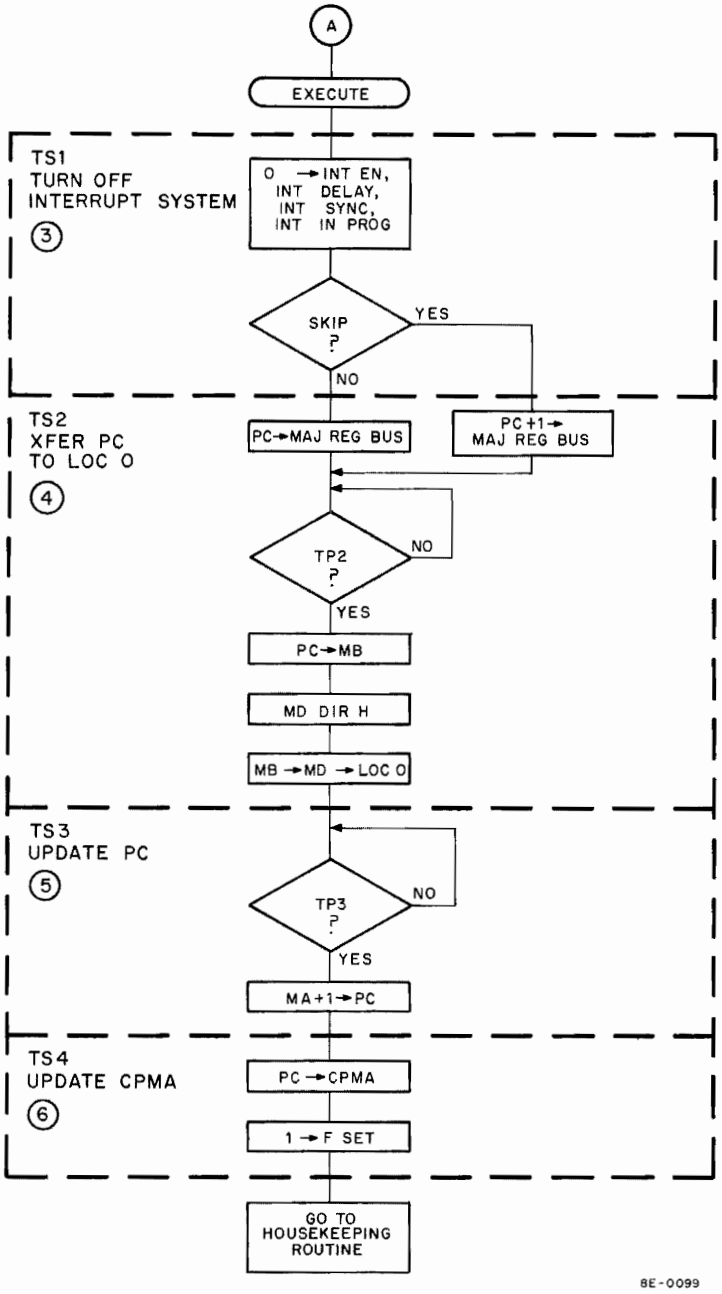

Figure 3-13 Programmed Interrupt System Flow Diagram (Sheet 2 of 2)

Flow Reference	Explanation
(4)	TRANSFER PC TO LOCATION 0 – The contents of the PC are transferred to location 0 during TS2. The Register Input Multiplexer is enabled to allow the contents of the PC to be applied to the MAJOR REGISTERS BUS (Figure 3-2). If the SKIP flip-flop is set, CAR IN is also asserted. At TP2, the content of the MAJOR REGISTERS BUS is loaded into the MB Register. Because MD DIR L is negated (H) at TP2, the content of the MB is immediately applied to the MD BUS, gated into the inhibit drivers, and routed to the addressed memory location (location 0).
(5)	UPDATE PC – During TS3, the content of the CPMA is gated through the Register Input Multiplexer and applied to the adders (Figure 3-2). A CAR IN L signal is developed that places a 1 on adder stage 11. The result is applied to the MAJOR REGISTERS BUS and loaded into the PC at TP3.
(6)	UPDATE CPMA – During TS4, the Register Input Multiplexer is enabled to allow the content of the PC to be applied to the MAJOR REGISTERS BUS and loaded into the CPMA at TP4. Because INT IN PROG is not active, F SET L will be asserted and the next processor cycle will be FETCH. In the event that any important data is in the AC and LINK, a housekeeping routine to store this data must be enacted.

3.9.6.1 Check Interrupt Request Line (SRQ) Instruction Flow Diagram – Refer to Figure 3-14 for the following discussion:

Flow Reference	Explanation
(1)	During TS1, the SKIP flip-flop is cleared. The content of the CPMA Register is gated through the Register Input Multiplexer (Figure 3-2) and placed on the adders. A 1 is developed by the Carry In logic and placed on the adder stage 11. The MA + 1 result is then loaded into the PC Register at TP1. The flow diagram assumes that the current addressed memory location contains instruction (6003) SRQ. READ memory begins during the latter portion of TS1.
(2)	During the second half of TS1 and the first half of TS2, the READ operation is active, and the content of the addressed memory location is read into the memory register (Figure 3-2). Because MD DIR L was asserted during TS1, the content of the memory register will be gated out to the MD BUS and ready for decoding. The Instruction Register looks at the first three bits (0–2) and decodes the IOT. I/O PAUSE L is generated earlier. I/O PAUSE L allows the IOT Decoder to decode the last three bits, providing the middle six bits are 0s. Because the last three bits contain 3_8 (for an SRQ instruction), the Interrupt Request line is now ready to be tested during TS3.
(3)	If an Interrupt Request has been made, signal SKIP L is asserted.
(4)	When SKIP L is asserted, CAR IN L is developed, and a 1 is placed on adder stage 11. The Register Input Multiplexer (Figure 3-2) is enabled so that the content of the PC is placed on the adders. The content of the PC + 1 is applied to the MAJOR REGISTERS BUS and loaded into the CPMA during TS4. If SKIP L was not asserted, only the PC is loaded into the CPMA, and the processor goes on to the next sequential instruction. Otherwise, a Flag Check subroutine is next performed.

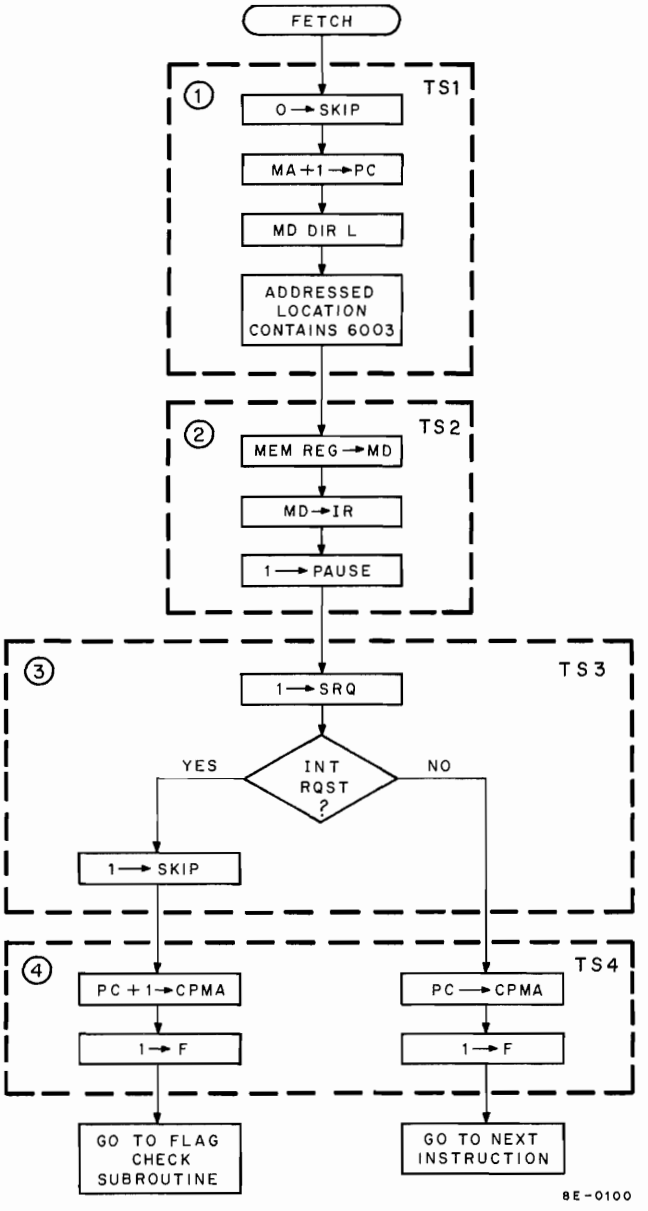

Figure 3-14 Check Interrupt Request Line Instruction Flow Diagram

3.9.6.2 Turn On Interrupt (ION) System – The Interrupt System is turned on during the restoration housekeeping routine (Figure 3-13). Refer to Figure 3-15 for the following discussion:

Flow Reference	Explanation
(1)	The SKIP flip-flop is cleared during TS1, and a 1 is added to the content of the CPMA and loaded into the PC.
(2)	With MD DIR L, the content of the addressed memory location is placed on the MD BUS during the READ operation. The instruction is applied to both the Instruction Register and the IOT Decoder.
(3)	The resulting ION instruction sets the INT EN flip-flop at TP3.
(4)	At TS4, the CPMA Register is updated and F SET L is enabled.

NOTE

During the cycle following TP1, INT DELAY is set; this ensures that the processor cannot honor an interrupt until the end of the next instruction.

3.9.7 JUMP Instruction

The JUMP instruction first modifies the PC and then modifies the CPMA so that both contain the new address at the start of the next instruction. A test is also made to determine if the instruction is direct addressed (the next processor cycle is FETCH), or if the instruction is indirectly addressed (the next processor cycle is DEFER). If the instruction is direct addressed, the content of the addressed memory location will be an instruction. If the address is indirect, the content of the addressed memory location will contain the address of the next instruction.

The JUMP instruction flow diagram is illustrated in Figure 3-16. This flow diagram is a subflow of Figure 3-8 and contains only the TS3 portion of the JUMP instruction.

If MD4 L = 1, PAGE Z L is not asserted (indicating that the new address will be on the current page). The first five CPMA output lines are routed through the Adder Output Multiplexer to the MAJOR REGISTERS BUS. Thus, the first five MA bits are gated through to the MAJOR REGISTERS BUS.

If MD4 L = 0, PAGE Z L is asserted; the first five MA bits are negated and cause 0s to be placed on the MAJOR REGISTERS BUS.

Because MD5 L – MD11 L output lines are routed directly to the Adder Output Multiplexer, these seven bits are applied to the MAJOR REGISTERS BUS. The content of the MAJOR REGISTERS BUS is then loaded into the PC at TP3, and a test for direct or indirect addressing is next accomplished. (Note that if JMP is indirect, the PC is loaded twice, once during FETCH, and the second time during DEFER. The first address is ignored.) The modification of the CPMA is accomplished in a similar manner (Figure 3-8).

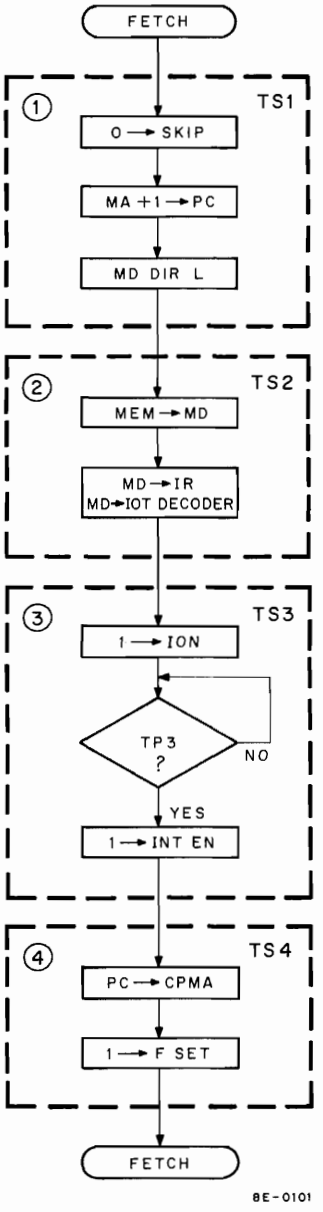

Figure 3-15 Turn On Interrupt (ION) System Flow Diagram

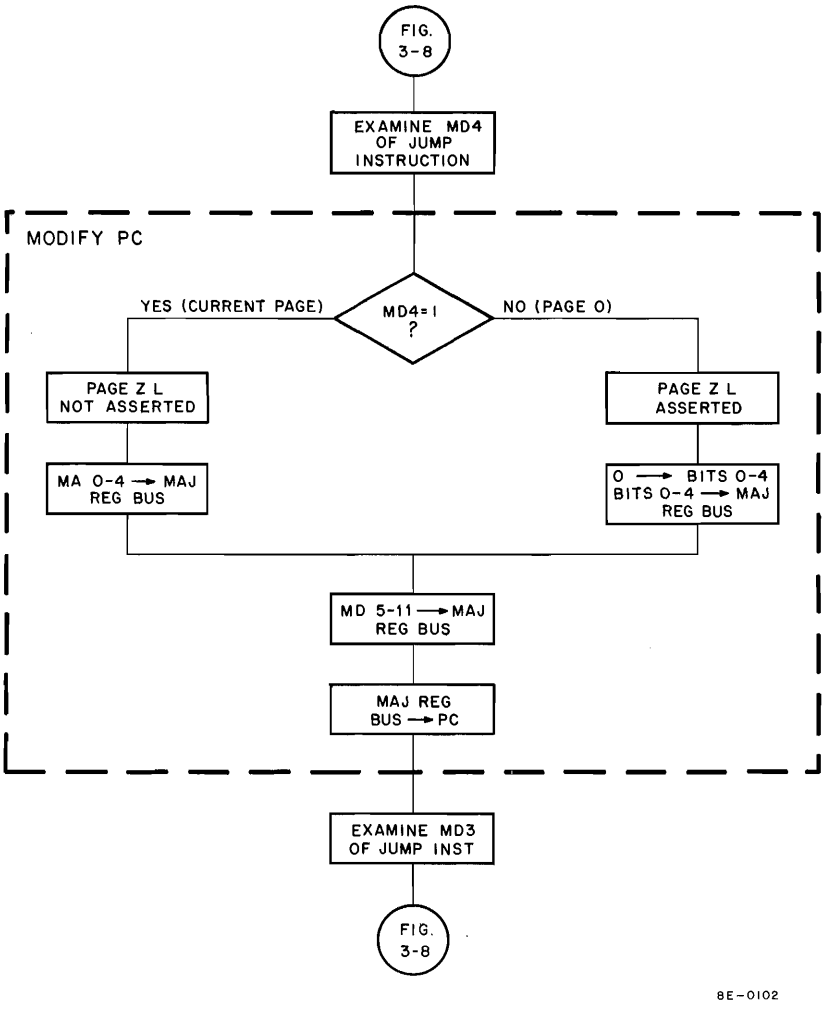

Figure 3-16 Direct JUMP Instruction Flow Diagram

3.10 DEFER STATE INSTRUCTION FLOW DIAGRAM

The DEFER state instruction flow diagram is illustrated in Figure 3-17. DEFER performs two types of functions. During any one processor cycle, DEFER provides an indirect address to the location containing the operand; if the addressed location is between 10_8 and 17_8, it provides the autoindex operation.

Flow Reference	Explanation
(1)	The DEFER state is always entered from the FETCH state, on indirect addressing. During the last half of TS1 and the first half of TS2, the content of the addressed memory location is read from memory and placed in the Memory Register (Figure 3-2). Because MD DIR L is asserted at this time, the content of the Memory Register is gated out to the MD BUS.
(2)	The content of the MD BUS is gated through the Register Input Multiplexer to the adders (Figure 3-2) using Register Input Enable Logic. At the same time, the Carry In logic places a 1 in the adders. The result is then placed on the MAJOR REGISTERS BUS and, at TP2, is loaded into the MB Register.

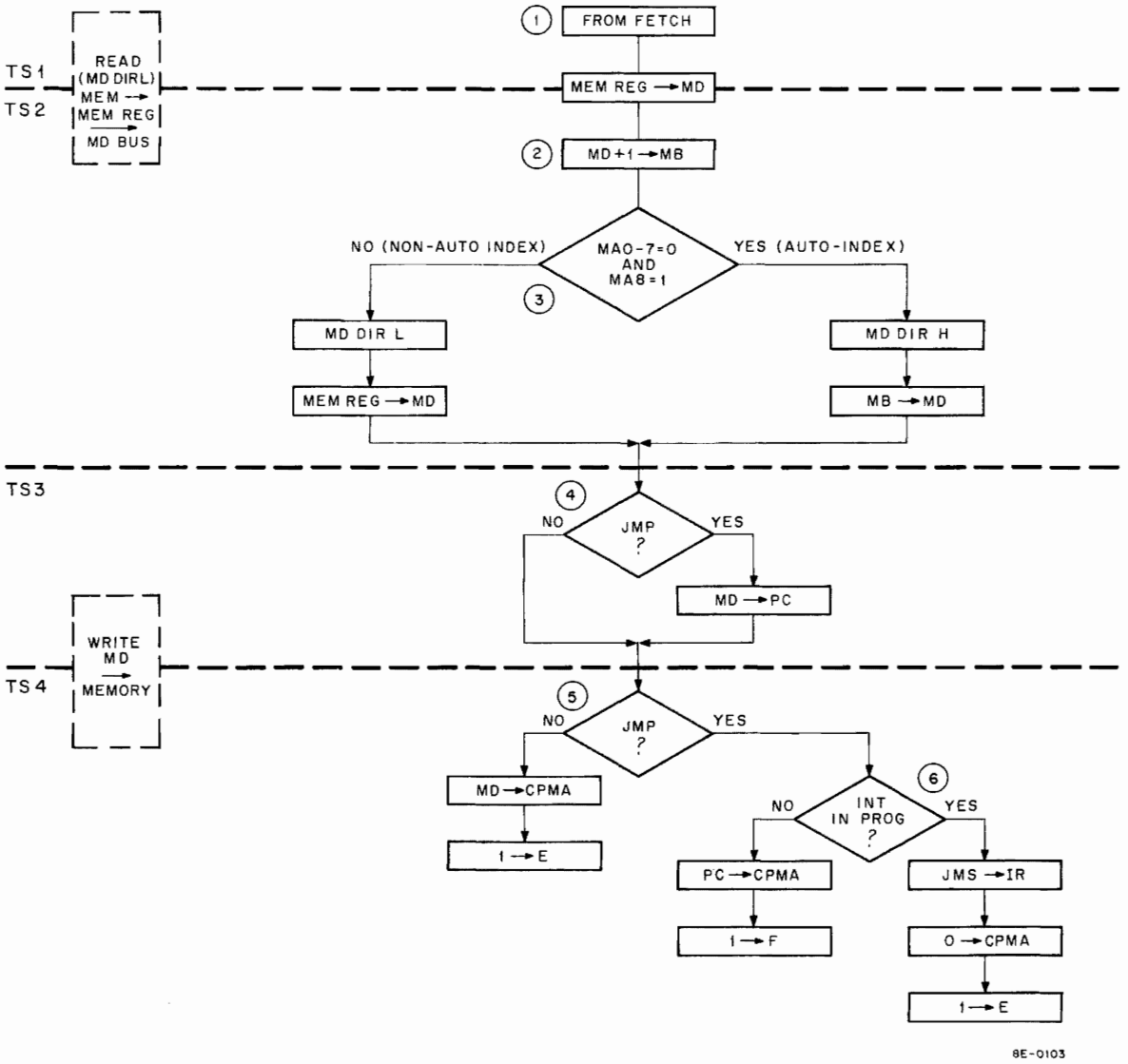

Figure 3-17 DEFER State Instruction Flow Diagram

Flow Reference	Explanation
(3)	The autoindex operation is determined by examining the content of the first nine Memory Address bits. If bits 0–7 contain 0s and bit 8 contains a 1, MD DIR L is allowed to go high and the content of the MB Register (which contains MD + 1) is gated onto the MD BUS. Otherwise, MD DIR L remains low and the content of the Memory Register is gated onto the MD BUS.
(4)	If the JMP instruction is in the IR, the content of the MD is gated through the Register Input Multiplexer, through the adders, onto the MAJOR REGISTERS BUS, and loaded into the PC at TP3. Remember the MD BUS carries either the previous memory contents (if the instruction is not autoindexed), or the incremented memory contents (if the instruction is autoindexed). If JUMP is not in the IR, then no action is taken during TS3, and JUMP is tested again in TS4.
(5)	If the JMP instruction is in the IR, the processor goes on to test the INT IN PROG line. Otherwise, the content of the MD BUS is again gated through the Register Input Multiplexer, through the adders, and onto the MAJOR REGISTERS BUS. At TP4, the CPMA is loaded containing the new address of the operand. The combination of DEFER and JMP does not necessarily cause the next processor state to be EXECUTE.
(6)	If the IR contains JMP, the INT IN PROG line is tested. If no interrupt has occurred, the content of the PC is gated through the Register Input Multiplexer, through the adders to the MAJOR REGISTERS BUS. At TP4, the CPMA is loaded. Because the current major state is DEFER and the instruction is JMP, the next major state must be FETCH. If there is an INT IN PROG, a JMS is forced into the Instruction Register, all 0s are forced into the CPMA, and the next major state is EXECUTE.

3.11 EXECUTE STATE INSTRUCTION FLOW DIAGRAM

The EXECUTE state instruction flow diagram is shown in Figure 3-18. EXECUTE can be entered from FETCH, DEFER, or EXECUTE. During the second half of TS1 and the first half of TS2, the READ operation is performed. MD DIR L is also asserted to allow the content of the addressed memory location to be gated out to the MD BUS (Figure 3-2).

Flow Reference	Explanation
(1)	The operation of the AND and TAD instructions is the same during TS2. The MD gate of the Register Input Multiplexer is enabled and the content of the MD BUS is placed on the MAJOR REGISTERS BUS. At TP2, MB LOAD L is developed and loads the content of the MAJOR REGISTERS BUS into the MB Register. Also at TP2, MD DIR L is allowed to go high and the content of the MB is automatically placed on the MD BUS. Although this operation does not change any register or bus during an AND or TAD instruction, it is automatic for both instructions during the EXECUTE state.

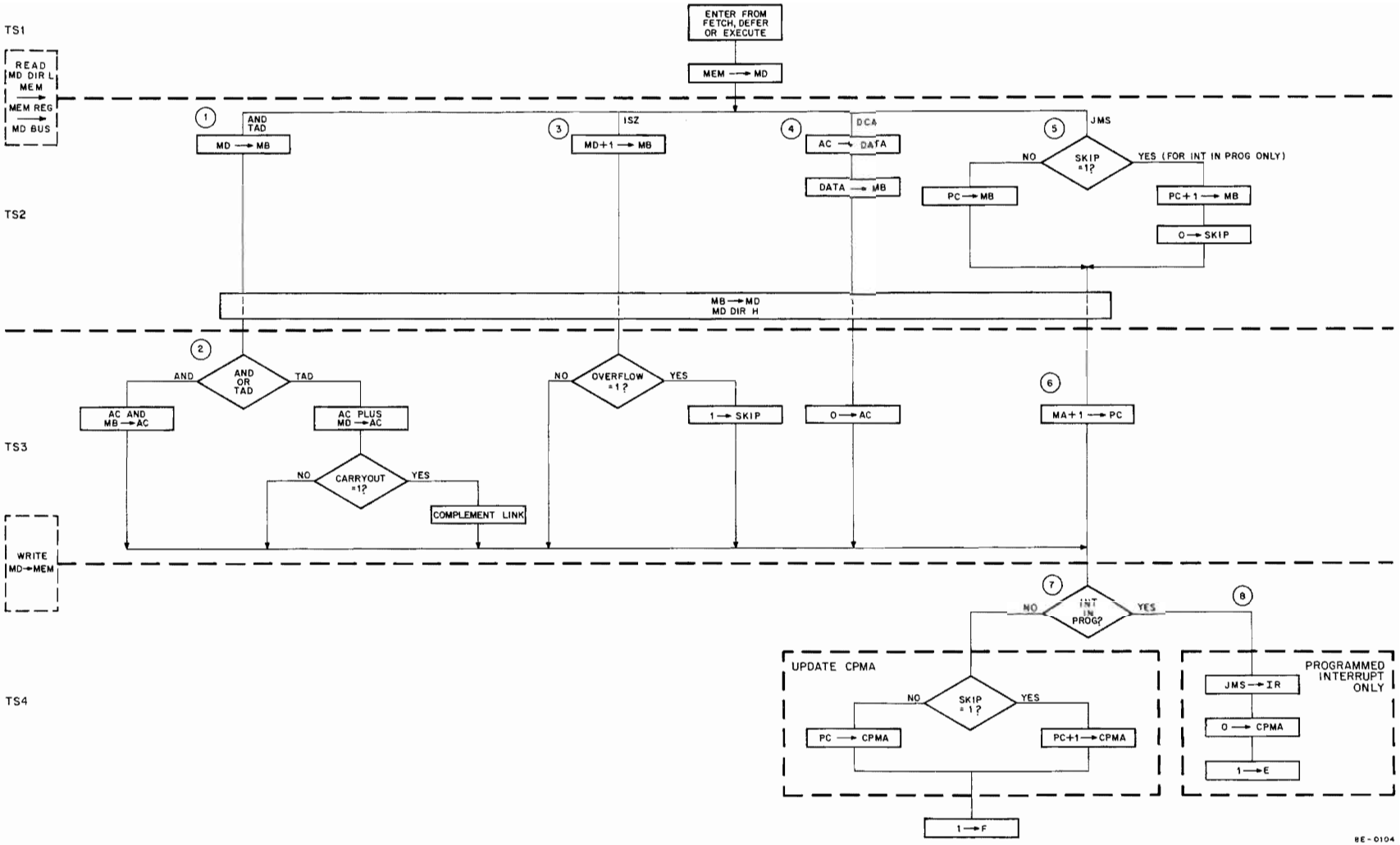

Figure 3-18 EXECUTE State Instruction Flow Diagram

Flow Reference	Explanation
(2)	If the instruction is AND, the AC/MB AND gate (Figure 3-2) receives the content of the AC and the MB. A logical AND function will be performed for each of the 12 bits; there is no carry from one stage to the next. The ANDed result is then applied to the Adder Output Multiplexer and placed on the MAJOR REGISTERS BUS. At TP3, the content of the MAJOR REGISTERS BUS is loaded into the AC. For a TAD instruction, the process differs. The Register Input Multiplexer is enabled to allow the content of the MD BUS to be applied to the adders. To bring the AC to the adders, enabling signal AC → BUS L is first developed. This places the content of the AC on the DATA BUS. To apply the content of the DATA BUS to the other side of the adders, the Data Control Gate (DATA T L) is enabled. The resulting addition is then applied to the MAJOR REGISTERS BUS and loaded into the AC at TP3. If CAR OUT L equals a 1, the result is applied to the Link Adder circuit, and the LINK is complemented.
(3)	If ISZ is in the Instruction Register, CAR IN L is asserted, which places a 1 in the adders at TS2. At the same time, the Register Input Multiplexer is enabled to allow the contents of the MD BUS to be placed onto the adders. If the OVERFLOW flip-flop is not set at TP2, no operation is performed during TS3. If the OVERFLOW flip-flop is set to 1, a 1 is developed on the SKIP line. (See Flow Reference (7) for CPMA Update.)
(4)	If instruction DCA is in the Instruction Register, signal AC → BUS L is developed, and the content of the AC Register is applied to the DATA BUS (Figure 3-2). The Data Control Gate is enabled next; thus, the content of the DATA BUS can be applied to the MAJOR REGISTERS BUS. At TP2, the content of the MAJOR REGISTERS BUS is then loaded into the MB Register and because MD DIR L goes high at TP2, the content of the MB Register is gated onto the MD BUS. To clear the AC, signal AC → BUS L is not asserted, and DATA T L is high. With DATA T L high, 0s are applied to the MAJOR REGISTERS BUS and loaded into the AC Register at TP3. The contents of the MD BUS are then applied to the inhibit drivers for the WRITE operation. WRITE begins during the second half of TS3 and continues through the first half of TS4.
(5)	If a JMS instruction is in the Instruction Register, the Register Input Multiplexer is enabled to allow the content to the PC to be applied through the adders to the MAJOR REGISTERS BUS and loaded into the MB Register at TP2. The SKIP L signal is also tested during TS2. If the Skip logic has produced a 1, SKIP L signal is applied to the Carry In logic, and signal CAR IN L becomes a 1*. This is applied to the adders and added to the content of the PC. The result is then applied to the MAJOR REGISTERS BUS and loaded into the MB at TP2. At TP2, the SKIP flip-flop is also cleared. (This condition can occur only when an interrupt is honored immediately after an OPR, IOT, or ISZ instruction.)
(6)	A CAR IN L signal is asserted and a 1 is placed in the adders. The content of the CPMA Register is gated through the Register Input Multiplexer to the adders. The result is applied to the MAJOR REGISTERS BUS and loaded into the PC Register at TP3.

*AC signal line is pulled low.

Flow Reference	Explanation
(7)	For all instructions, if there is no INTERRUPT IN PROGRESS, the SKIP L signal line is tested. If SKIP L does not equal 1, no CAR IN L signal is developed and the content of the PC Register is gated through the Register Input Multiplexer and then applied to the MAJOR REGISTERS BUS. At TP4, the content of the BUS is loaded into the CPMA Register. If the SKIP L signal equals 1 (because of ISZ and CARRY OUT), a CAR IN L signal is developed and applied to the adders. This signal is added to the PC and loaded into the CPMA at TP4. In both cases, F SET L is asserted and the next major state is FETCH.
(8)	If there is an INTERRUPT IN PROGRESS, a JMS instruction is forced into the Instruction Register and the Register Input Multiplexer is enabled so that 0s are applied to the MAJOR REGISTERS BUS. During TP4, the content of the BUS is loaded into the CPMA and EXECUTE is clocked into the Major States Register.