3. SYSTEM DESCRIPTION

This Chapter contains a description of the 3040 Controller and is presented in terms of the registers whose contents control the Controller operation and provide information to the CPU, and the instructions which control those registers.

Figure 3-1 is a block diagram of the 3040 Controller interfaced with a PDP-8 and a single disk drive. Using programmed I/O instructions, information moves to or from the Control Register, the Status Register, the Track Address Register, and the Sector Address Register; only to the Seek Address Register, and only from the Seek Status Register. The two buffer interface registers are connected to the DMA (Direct Memory Access) facility of the PDP 8 for data transfers and the Current Address Register is attached to the DMA facility for specifying the locations in the CPU memory to (or from) which the data is to be transferred.

REGISTER DESCRIPTIONS

The following controller registers are those with which the programmer has direct contact (either establishing or interogating their contents):

- Control Register

The Control Register (12 bits) contains the busy and done flags to indicate the current status of a controller operation, the disk unit select bits used to select one of the four ports for a data transfer, the extended memory address field for DMA transfers, the interrupt and format enable bits, and a read disk bit to indicate the direction of the DMA transfer taking place. The specific bit assignments are as follows:

BIT	FUNCTION
0,1,2	Extended Memory Address: Contains the three most significant bits of the computer memory address for DMA transfers.
3,4	Unused: Will always read as zeros.
5	Interrupt Enable: When set, this bit will enable the controller to generate an interrupt request when the done bit gets set.
6	Format Enable: When set, this bit will allow a sector to be formatted.
7,8	Disk Unit Select: A two bit field selecting one of four ports for a data transfer.
9	Read Disk Enable: This bit, which is automatically controlled by the controller, is used to indicate the direction of a data transfer. When set the controller is reading from the disk and when clear, the controller is writing onto the disk.
10	Busy Flag: Indicates the controller is busy transferring data to or from the selected disk.
11	Done Flag: When set, this bit indicates that either (1) a data transfer operation has been completed or (2) an independent seek operation has been completed while there is no data transfer active to any of the other three ports.

Status Register

The Status Register (12 bits) includes seven error-indicator bits and two disk-operation bits. A total of nine errors are sensed by the controller. They have been divided into three equal groups so that a two-bit field may describe which of the three errors has occurred or that none of the three has occurred. The complete bit assignments are as follows:

BIT		FUNCTION
0		Error Flag. Indicates that an error occurred.
1,2	00	No Format, Select, or Timing Errors.
	01	Format Error. Indicates an attempt to format a disk without having the format switch in the FORMAT position, or to format a fixed-head disk.
	10	Select Error. Disk command assigned to a port that either has no disk or has a disk which is not in a condition to operate.
	11	Timing Error. Computer did not respond in time to receive or supply a data word from/to the Controller.
3,4	00	No Logical Address Interlock, Address Verification or Seek Incomplete Errors.
	01	Logical Address Interlock. Indicates that the track address given to the Controller is greater than the maximum track value for the disk selected.
	10	Address Verification Error: Indicates that the Controller has detected a difference between the Track Address Word in the sector it is attempting to read or write and the track address it expects to find there. The Controller initiates an automatic restore on that disk.
	11	Seek Incomplete Error: Indicates a hardware malfunction in the disk. The Controller initiates an automatic restore on that disk.
5,6	00	No Write Lock Out, Write Check or Cyclic Redundancy Check Errors.
	01	Write Lock Out Error: Indicates an error occurred when the program attempted to write onto a write-protected sector. The format switch can override the write-protect capability in the moving-head disk.
	10	Write Check Error: Indicates a malfunction in the disk that makes it incapable of writing data.
	11	Cyclic Redundancy Check Error: Indicates that an error was detected in the cyclic redundancy check word when reading back the data from the disk.
7,8,9		Unused: Will always read as zeros.
10		Busy Flag: Same bit as in the Control Register.
11		Done Flag: Same bit as in the Control Register.

Seek Status Register

The Seek Status Register, used to hold the status and results of all seek operations, is composed of four 3-bit registers, each of which is associated with a disk port. In each 3-bit register, two bits are used to indicate the results of the last seek on the port while the third bit is a dynamic indication of whether the port is ready to receive a seek command. This register may only be read back to the accumulator, while the two bits used to indicate the seek results are automatically cleared upon a seek being initiated on that port. Those ports not having disks connected to them will have their 3 bit register read back as a 7_8. The complete bit assignments are as follows:

BIT	FUNCTION
0-2	Status register corresponding to disk port 3.
3-5	Status register corresponding to disk port 2.
6-8	Status register corresponding to disk port 1.
9-11	Status register corresponding to disk port 0.
0,3,6.9	Indicates that a Hardware Seek Error has occurred. This can occur from either seeking to a non-existent cyclinder (i.e., a Logical Address Interlock Error) or if the disk was unsuccessful in seeking to a legal cyclinder number (i.e., a Seek Incomplete Error). If a Seek Incomplete does occur, the controller will automatically generate a restore command to the disk.
1,4,7,10	Indicates that a Busy Error has occurred. This can occur from initiating a seek on a port when it was either active doing a data transfer or was not in a condition to receive a seek operation. In either case, the seek command is ignored when this error occurs.
2,5,8,11	A dynamic indicator for whether the port is in a condition to receive a seek command. A zero indicates it is ready while a one indicates that either the head is presently moving or that the drive in not ready.

- Seek Address Register

The Seek Address Register is a 12-bit register used to temporarily hold the port and cylinder address while an overlap seek is initiated. It is also used as a communication path for those program I/O instructions entering the Track Address Register. The Seek Address Register may not be read back into the accumulator, and is always free to receive programmed information without any timing restrictions. The specific bit assignments are as follows:

BIT	FUNCTION
0,1	A two-bit field used to select the port on which the overlap seek operation is to be initiated.
2-11	The track address to which the head will move when the overlap seek is executed. This track address is composed of a cylinder address (bits 2-10) and a head select bit (bit 11) for moveable-head disks and is a straight track address for fixed-head disks.

- Track Address Register

The Track Address Register is a 12-bit register used to hold the track address for read and write operations. It is entered with the starting track address when the read or write operation is initiated, and is automatically updated when data transfers require going across track boundaries. The specific bit assignments are as follows:

BIT	FUNCTION
0	Unused: Will always be read as a zero.
1	Disk Select: A zero will select the non-removeable disk and a one will select the removeable disk for a moveable-head disk. This bit should be a zero for the fixed-head disk.
2-11	The track address to or from which the controller will transfer data. This track address is composed of a cylinder address (bits 2-10) and a head select bit (bit 11) for moveable disks and a straight track address for fixed-head disks.

- Sector Address Register

The Sector Address Register is used to hold the sector address for read and write operations. It is a 4-bit register which is loaded with the starting sector address prior to the initiation of the read or write operation, and is automatically updated for data transfers which require going across sector boundaries.

BIT	FUNCTION
0-7	Unused: Will always be read as zeros.
8-11	Sector Address: A four-bit field which provides 16 sectors per track.

The 4-bit Sector Address Register should be viewed as the least significant part of continuous disk address, where the Track Address Register is the most significant part. Thus, when the automatic updating increments the Sector Address Register back to zero, it will also increment the least significant (head select) bit of the Track Address Register. With this addressing scheme, only multi-sector transfers going across cyclinder boundaries will loose a revolution while the head moves.

OTHER REGISTERS

The registers described below are also used by the 3040 controller, but are not available to programmer contact.

- Word Count Register

This 12-bit register stores the number of words remaining to be transferred and is updated as the transfer of each word takes place.

- Current Address Register

This 12-bit register holds the 12 least significant bits of the core memory address for the word being transferred and is incremented after each transfer occurs.

Data Shift Register

During a read operation the Data Shift Register takes the data from the disk in a bit-serial fashion (least significant bit first) and when a complete word has been assembled that word is transferred in parallel to one of the buffer interface registers. The transfers alternate between Buffer Interface Register #1 and Buffer Interface Register #2. During a write operation, data from the buffer interface registers are alternately transferred a word at a time into the Data Shift Register which in turn transmits the data in a bit-serial fashion (least significant bit first) out to the disk.

Buffer Interface Register

As mentioned above, the data coming from the disk to the computer or vice versa pass through one of the two buffer interface registers. For a sequence of words being transferred, the registers are used alternately (first Register #1, then Register #2, then Register #1 and so on). This double buffering scheme gives the computer twice the one-word transfer time to respond to a data transfer request. With the high bit-transfer rates of these disk drives, this is particularly important if time-consuming instructions, such as indirect addressing sequences, are being used.

Arithmetic Check Register

This register accumulates the arithmetic checksum word generated during the transfer of data to or from a sector. After a write operation this word is written at the end of each sector. After a read operation, the previously written checksum word is compared to the contents of this register to verify the correctness of the data transfer operation.

- Sector Counter

  This register contains the number of the sector currently under the read/write heads. As the disk revolves, the Sector Counter is updated by the sector pulses from the disk and is compared with the contents of the Sector Address Register in order to determine when a data transfer operation should begin. This counter is located in the disk drive for moveable-head drives and on the disk interface cable for fixed-head drives.

DISK SECTOR FORMAT

This section describes the format of each sector on the cartridge disks and the fixed-head disks.

Moveable-Head Disk Sector Format

The format for a moveable-head disk sector is illustrated in Figure 3-2. Each item in this sector is described below.

- First Preamble

  The preamble at the beginning of each sector consists of twenty 12-bit words written on the disk. The first 239 bits in the preamble are zeros; the last bit is a one.

- Track Address Word

  This 12-bit word written on the disk contains the track address of the particular sector. The track address is written on a cartridge when it is formatted. Before a data transfer operation takes place, this track address is read and compared with the desired address in order to verify that the correct track has been located. Bits 1-11 of the

Track Address Word must correspond directly with bits 1-11 of the Track Address Register for the verify to be completed. Bit 0 of the Track Address Word is used as the write protect bit for the sector. If it is a zero, normal operation will occur. It it is set to a one, the sector will be write-protected and a write lock out error will occur if an attempt is made to write in a write-protected sector. Placing the format switch in the "FORMAT" position will override this write protect bit and allow updating of data in a write-protected sector.

- Second Preamble

  The Second Preamble contains a 51.2 us string of bits (all zeros except for the last bit which is a one). This preamble envelopes the write amplifier turn-off and turn-on for the format and data sections respectively, and provides the read circuitry with a zero field for resynchronization during a read operation.

- Data

  The data portion of the sector contains 256 12-bit words.

- Cyclic Redundancy Check Word

  This 12-bit word is the one's complement sum of the 256 data words in the sector. This word is automatically computed by the controller and written on the disk during a write operation. It is read and compared with a recalculated value from the disk data to verify the validating of the data transfer during a read operation.

- Overhead

  The overhead is the unused portion of the sector. It is nomially 157us, but will vary as a function of the instantaneous speed tolerances of the disks and with interchangability tolerances of the disk cartridges.

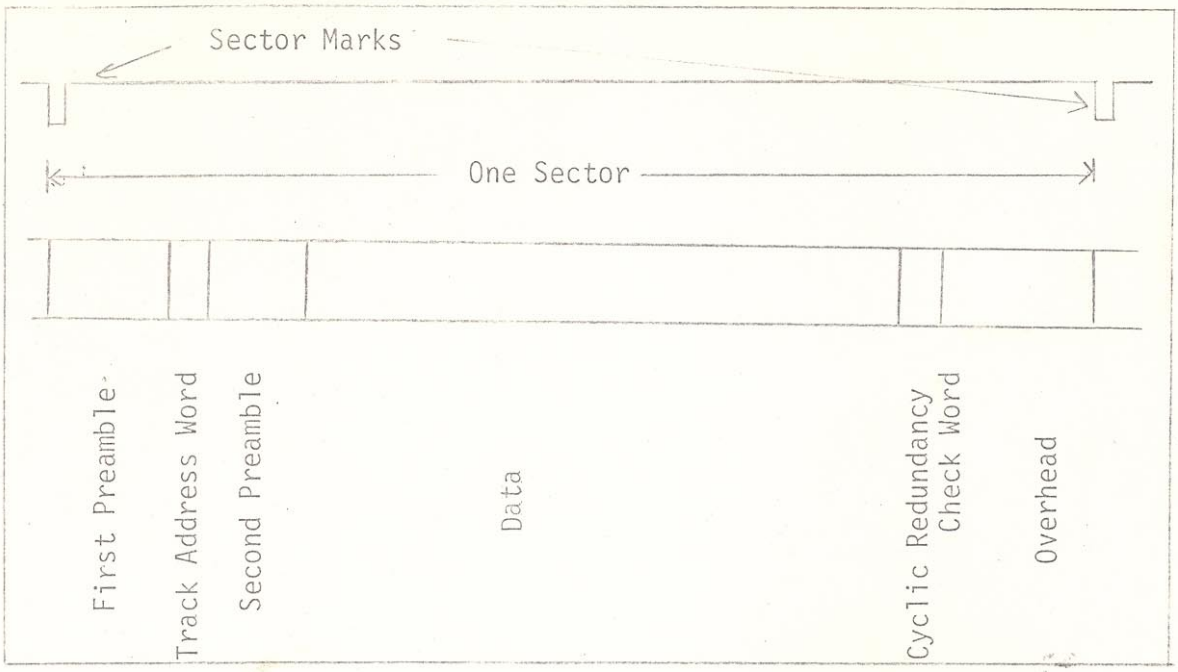


Figure 3.2 Moveable-head disk Sector Format

Fixed-Head Disk Sector Format

The format for a fixed-head disk sector is illustrated in Figure 3.3. Each item in this sector is described below.

- Preamble

  The preamble at the beginning of each sector consists of nine bits. The first seven bits are ones followed by a zero-one combination for the last two bits.

- Data

  The data portion of the sector contains 256 12-bit words.

- Cyclic Redundancy Check Word

  This 12-bit word is the one's complement sum of the 256 data words in the sector. This word is automatically computed by the controller and written on the disk during a write operation. It is read and compared with a recalculated value from the disk data to verify the validity of the data transfer during a read operation.

- Overhead

The overhead is the unused portion of the sector. It has a nominal value of 20 us.

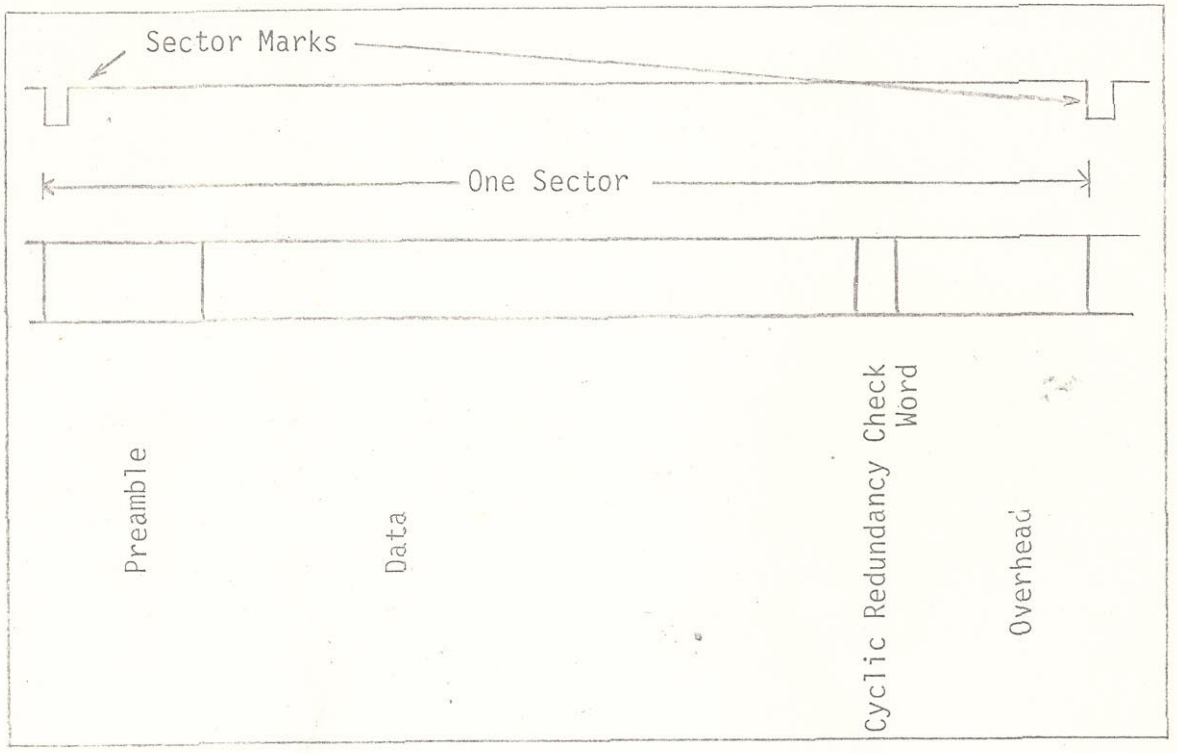


Figure 3.3 Fixed-Head Disk Sector Format

*NOTE: The formatting of the fixed-head disk is done by the writing of a clock track on the disk with special equipment.

DISK CONTROLLER INSTRUCTIONS

This section describes the instructions used to specify the operations of Model 3040 Controller when they are interfaced to a PDP 8 Series computer. These instructions are used for both moving-head and fixed-head disks. Table 3-1 summarizes the instructions and their functions.

Table 3-1

Model 3040 Disk Controller Instructions for the PDP 8 Series Computer

Instruction	Octal Equivalent*	Function
DSDD	6501	Skip on Disk Done.
DLCR	6502	Load Control Register
DRCR	6503	Read Control Register
DCSR	6504	Clear Status Register
DRSR	6505	Read Status Register
DLSS	6506	Load Seek Address Register and Initiate Overlap Seek
DRSS	6507	Read Seek Status Register
DSDE	6511	Skip on Disk Error
DLSR	6512	Load Sector Address Register
DSRR	6513	Read Sector Address Register
DLTR	6514	Load Track Address Register and Initiate Read
DLTW	6515	Load Track Address Register and Initiate Write
DRTR	6516	Read Track Address Register
DWCA	6517	Initiate Word Count and Current Address Sequence

* The use of the standard device codes 50_8 and 51_8 for the Model 3040 Controller.

Instruction: DSDD (Octal Code: 6501)
Skip On Disk Done

This instruction causes the computer to skip the next instruction whenever the done flag (bit 11 of either the Control Register or the Status Register) is set in the controller.

Instruction: DLCR (Octal Code: 6502)
Load Control Register

This instruction transfers the contents of the accumulator into the Control Register. It is used to initialize the Control Register prior to a data transfer, particularly the extended memory address, interrupt enable and format enable bits.

Instruction: DRCR (Octal Code: 6503)
Read Control Register

This instruction clears the accumulator and then transfers the contents of the Control Register into the accumulator.

Instruction: DCSR (Octal Code: 6504)
Clear Status Register

This instruction clears all the bits in the Status Register in the controller.

Instruction: DRSR (Octal Code: 6505)
Read Status Register

This instruction clears the accumulator and then transfers the contents of the Status Register into the Accumulator.

Instruction: DLSS (Octal Code: 6506)
Load Seek Address Register and Initiate Overlap Seek

This instruction transfers the contents of the accumulator into the Seek Address Register and initiates an overlap seek (a head movement without a following data transfer) to the disk port specified by bits 0 and 1 and to the track specified by bits 2-11. This instruction can be initiated at any time and will be ignored if on that port, another seek or a data transfer is currently being executed.

Instruction: DRSS (Octal Code: 6507)
Read Seek Status Register

This instruction clears the accumulator and then transfers the contents of the Seek Status Register into the accumulator. The individual 3-bit registers for each port combine to make a 12-bit transfer with bits 0-2, 3-5, 6-8, and 9-11 corresponding to disk ports 3, 2, 1 and 0 respectively.

Instruction: DSDE (Octal Code: 6511)
Skip on Disk Error

This instruction causes the computer to skip the next instruction whenever the error flag (bit 0 of the Status Register) is set in the controller.

Instruction: DLSR (Octal Code: 6512)
Load Sector Address Register

This instruction transfers the least significant 4 bits (bits 8-11) of the accumulator into the Sector Address Register.

Instruction: DSRR (Octal Code: 6513)
Read Sector Address Register

This instruction clears the accumulator and then transfers the Sector Address Register into bits 8-11 of the accumulator.

Instruction: DLTR (Octal Code: 6514)
Load Track Address Register and Initiate Read

This instruction transfers the contents of the accumulator into the Track Address Register and initiates the following sequence:

(1) A seek is initiated to the track specified by bits 1-11 of the Track Address Register on the disk port specified by bits 7 and 8 of the Control Register.

(2) When the track and sector are reached, the controller goes through an address verification sequence where it verifies that the correct track has been reached by reading the Track Address Word and comparing it with the contents of the Track Address Register. This verification sequence is done only for moving-head disks to verify the head movements, and is not needed to verify the electronic head selection circuitry of the fixed-head disks.

(3) After the verification sequence is done (if needed) the read sequence will commence where the controller will convert the serial data on the disk into parallel 12 bit words and transfer them into core using the Current Address Register as the pointer as to where to store each word in core.

(4) The read operation will continue until the number of words initially specified in the Word Count Register has been transferred. As the data is read in from each sector on the disk, a one's complement sum is calculated from the data and compared with the cyclic redundancy check word in that sector to verify the validity of the data.

(5) The controller operates on total sector each time but transfers only the initial Word Count Register number of words into core. Should the initial value be less than or equal to a sector length, the read operation will terminate at the end of the initial sector after checking the validity of the data. Should the initial value be greater than a sector length, the read operation will go automatically from sector to sector (checking for address verification on each sector if necessary) and will cross both track and cyclinder boundaries until the initial Word Count Register value of words has been transferred.

NOTE: For moveable-head disks, it will take an additional revolution when reading across cyclinder boundaries to allow time for the heads to move. Except for this case, all large transfers will go from sector to sector without losing any time between sectors.

(6) As each sector is read successfully, the disk address (viewed as a 15 bit register composed of bits 1-11 of the Track Address Register as the most significant part and the Sector Address Register as the least significant part) is incremented to point to the next sector. Thus, at the conclusion of the data transfer, the disk address will point to the sector immediately following the last sector read if the transfer terminated successfully.

(7) At the conclusion of the data transfer or whenever an error has been sensed, the Done Flag will be set and an interrupt request to the computer will be generated if the Interrupt Enable Bit (bit 5 of the Control Register) is set.

Instruction: DLTW (Octal Code: 6515)
Load Track Address Register and Initiate Write

This instruction transfers the contents of the accumulator into the Track Address Register and Initiates a WRITE sequence. These are the same set of sequences as the READ instruction with the following exceptions:

- In the address verification sequence, the most significant bit of the Track Address Word is tested to see if the sector is write-protected. Trying to write into a write-protected sector will terminate the write operation and set both bits 0 and 6 in the Status Register.
- The write operation will transfer words from core to the disk until the initial value of the Word Count Register has been reached. It will then write the remaining words in the sector (should there be any) as zeros.

- While it is transferring data to each sector, the controller computes the one's complement sum of the data in the sector and then writes this value as the Cyclic Redundancy Check Word immediately after the data in each sector.

Instruction: DRTR (Octal: 6516)
Read Track Address Register

This instruction clears the accumulator and then transfers the bits 1-11 of the Track Address Register into the accumulator.

Instruction: DWCA (Octal Code: 6517)
Initiate Word Count and Current Address Sequence

This instruction will transfer the contents of the accumulator into the Seek Address Register and initiate the following sequence:

(1) The controller interprets the information in the Seek Address Register as an address and transfers this information into the Current Address Register.

(2) It then uses this address plus the Extended Memory Address (bits 0-2 of the Control Register) as a pointer and initiates a two word DMA sequence.

(3) The first word retrieved is interpreted as the initial word count for the ensuing data buffer and is transferred into the Word Count Register.

(4) The second word retreived is interpreted as the intial core address for the ensuing data buffer and is transferred into the Current Address Register.

The following information is provided to help the user better understand the Model 3040 Controller and aid in its' programming.

- Master Clear

  The Model 3040 Controller contains its own master clear generator circuit and also receives the master clear signal of the Program I/O bus. The master clear function clears the Status Register, the interrupt enable, format enable, busy and done bits in the Control Register, the busy and hardware error bits in each of the Seek Status Registers and all sequence control status in the controller necessary to initialize the controller.

- The Overlap Seek and The Seek Status Register

  The purpose of the Seek Address and Seek Status Registers is to give the Model 4400/4500 Disk Systems a true overlap seek capability, which is independent of whether a data transfer is in progress on another port. An overlap seek is initiated by the execution of the DLSS instruction. There bits 0 and 1 of the Seek Address Register define which of the four disk ports the seek is to take place on, and bits 2-11 define the cyclinder and head-select (i.e., the track address) to which the heads should be moved to. The Disk Select Bit, bit 1 of the Track Address Register, does not need to be defined for the overlap seek operation since all four heads in the moving-head disk drive are attached to the same head positioner mechanism. The overlap seek capability can be used even in a single disk drive system, since any read or write initiation will be automatically queued in the controller until the port on which the data transfer is to take place

becomes ready. This queue also alleviates any timing restrictions on when to initiate a read or write sequence.

The completion of an overlap seek on any port will set the done flag in both the Status and Control Register, if and only if a data transfer is not active at that time. A program interrupt will also be generated if interrupts are enabled at the time the done flag gets set. Should any overlap seek operations terminate during a data transfer on another port, this fact will not be identified to the program at that time, and it will be up to the user to interrogate the Seek Status Register (bits 2, 5, 8, and 11 for ports 3, 2, 1, and 0 respectively) to determine if any other head movements did terminate during the data transfer should this information be needed.

The hardware will automatically protect against the initiation of overlap seeks if the port in question is presently either active with a data transfer or has its head moving and is not in a condition to enact another seek. In both these cases, the seek initiation is ignored and the busy error bit in that port's Seek Status Register is set.

- The Control and Status Registers

Except for the done flags capability of being set at the end of an overlap seek, both the Control and Status Registers are used exclusively for data transfers. The Status Register, which contains any error information resulting from a data transfer along with the redundant busy and error flags, can have the error portion cleared only by program control and set only by the controller upon the detection of any of the nine errors. This register should be cleared

prior to a data transfer initiation, so that any information in it after the data transfer can be only a result of that data transfer.

The Control Register contains both control and status information for data transfer operations. Bits 0, 1, and 2 comprise the Extended Memory Address field, which are the three most significant bits of the 15-bit (32K address ability) memory address used for all DMA transfers. The four bits comprising the interrupt enable, format enable and disk unit select bits must be appropriately set by the programmer according to their usage. However, while read disk, busy and done flags may be set or cleared by a DLCR instruction, they are also under automatic control of the controller. The read disk bit is used to control the direction of DMA transfers and must be controlled for both the word count/current address sequence as well as the read or write operations. The busy flag is automatically set at the time of a DLTR or DLTW instruction and cleared when the data transfer terminates. The done flag will automatically be cleared (if it is not already) at the time of a DLTR or DLTW instruction and will be set when the data transfer terminates.

- Word Count/Current Address Sequence

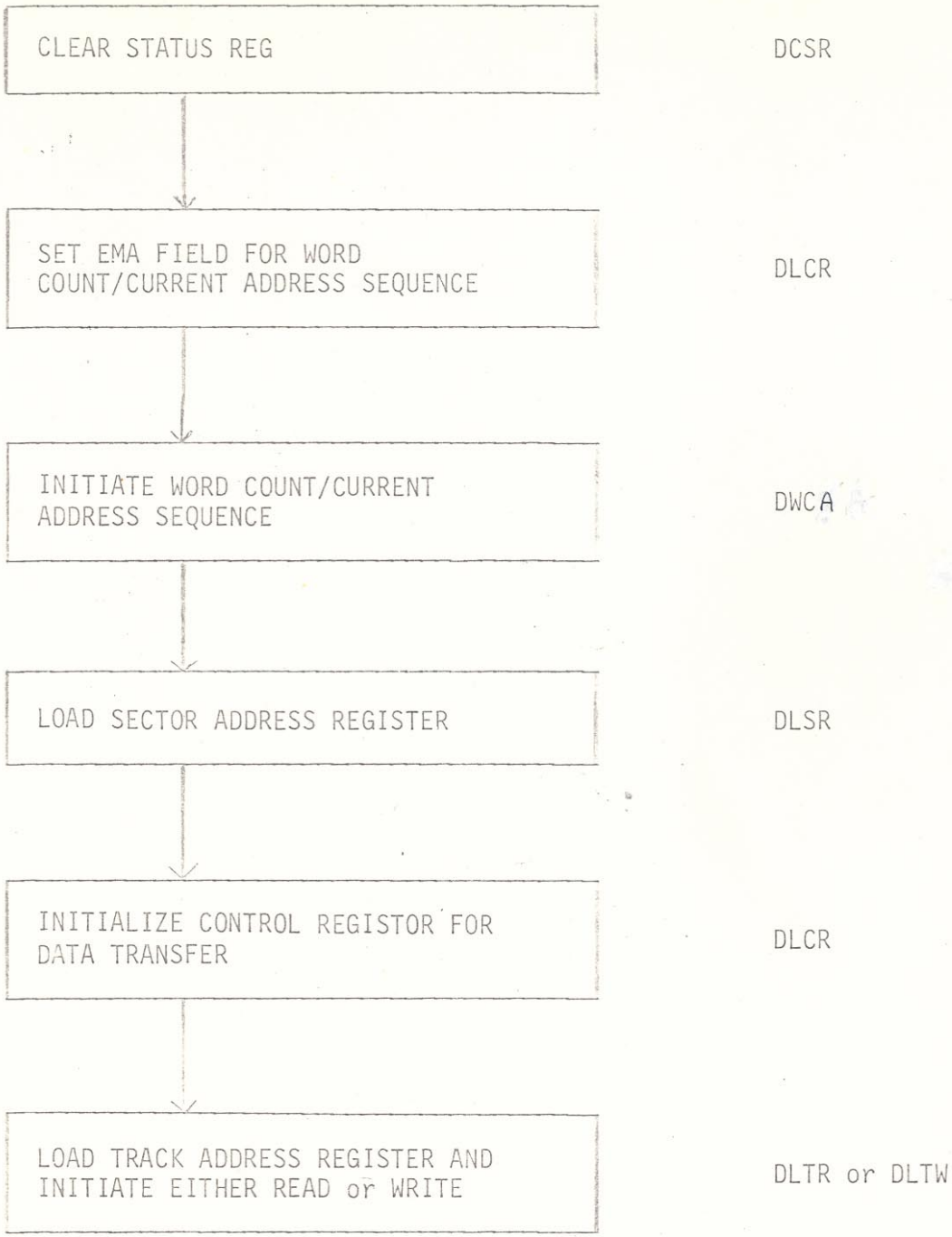
The word count/current address sequence was designed to allow the user to initialize two of the three basic parameters needed to initiate a data transfer with one programmed I/O instruction. The controller interprets the information transferred during a DWCA instruction as the address of the first of two consecutive words in core, and initiates a two word DMA sequence to retrieve them. This will require that the Extended Memory Address field in the Control Register must point to the 4K memory bank in which the word count and current

address parameters reside prior to the DWCA instruction. Should the ensuing data transfer be to or from a different 4K memory bank, the Extended Memory Address field must be reset prior to the DLTR or DLTW instructions. The word count register is a 12-bit register and allows for a full 4096 word transfer from a single data transfer initiation. The Extended Memory Address field is not capable of being incremented, so that any transfer incrementing the 12-bit current address Register past its maximum value will wrap around to the beginning of 4K memory bank pointed to by the Extended Memory Address field.

- Read or Write Operations

The design concept of the Model 3040 Controller was to minimize the programming sequence needed to set up and initiate a data transfer and have this one sequence capable of transferring from 1 word to 4096 words without regard to any disk boundaries. The controller utilizes two consecutive device code numbers for its instruction set and these numbers are selectable to be any two consecutive numbers starting with an even number. Also for PDP-8E or M or F computers, the DMA priority is normally set to level 1, although any of the other eleven levels may be selected.

The sequence to initiate a data transfer is described by the following flow diagram along with the I/O instruction mnemonic used to accompish each action:



As seen from this flow diagram, the same sequence is used for both read and write operations with the only difference being whether a DLTR or DLTW instruction is used. Program written to operate in only 4K of memory don't need the second DLCR instruction.

Data Transfer Monitoring

The Model 3040 Controller is designed to utilize both the skip on done and interrupt capabilities of the computer. Thus once the data transfer has been initiated, the user may periodically test for the completion of the data transfer by executing a DSDD instruction with the result of skipping the next program instruction if the data transfer is completed. If the user chooses not to periodically test for the data transfer completion, he may set the interrupt enable bit at the time he initializes the Control Register for the data transfer, which will result in an interrupt generation upon the completion of the data transfer.

If the interrupt method is chosen, the interrupt routine must first poll all devices to see which device has interrupted. Once the controller has been identified as the interrupting device, or if the periodic done flag testing was used to determine the data transfer completion, the skip-on-error instruction, DSDE, can be used to test if any errors occurred during the data transfer. If any error did occur, the description of the error can be obtained by interrogating bits 1-6 of the Status Register.

The action taken by the program in case of errors will depend on the specific application. However, certain errors may allow recovery techniques while others are invariably fatal. Address Verification, Write Check, Cyclic Redundancy Check, Timing, and Seek Incomplete errors may sometimes be corrected by repeating the current operation (which includes reinitializing the Control and Status Registers). If the error is a recoverable one, it will not persist for more than seven attempts. Beyond seven attempts, it should be considered fatal.

If the interrupt scheme was used, the programmer should clear the done flag prior to the execution of an ION instruction to prevent any false interrupts from occurring.

- Disk Formatting

Before data can be written onto a moving-head disk sector, and hence read from the sector, the sector must be formatted by writing a preamble and Track Address Word at the beginning of each sector. This is accomplished by initiating a write sequence, the same sequence as if writing data except for the following conditions:

1) The format switch must be manually placed in the FORMAT position.
2) The format enable bit (bit 6 of the Control Register)must be set to a one.
3) The word count must be specified as 25_8 (21_{10}).
4) The data buffer must be following:
   a) the first 23_8 (19_{10}) words must be zero.
   b) the 24_8 (20_{10}) word must be 4000_8.
   c) the last word of the data buffer is the Track Address Word.

Thus, each sector is formatted separately by initiating a write sequence with the above special requirements. It will result in a string of 239 zeros being placed on the disk starting at the sector notch with a one being written on the disk in the 240th bit time (96us). The twelve bits immediately following the single one bit will be the Track Address Word.

Track Address Word and Sector Write Protection

The last word of the data buffer when formatting a sector is the Track Address Word. For normal operation (i.e., not write-protecting a sector) the most significant bit of this word should be a zero and bits 1-11 are identical to the bits 1-11 which were loaded into the Track Address Register when the write sequence was initiated to format the sector. If it is desired to format the sector in the write-protect mode, the most significant bit (bit 0) of the Track Address Word must be set to a one. Once it is formatted in the write-protect mode, data may be written into the sector by leaving the format switch in the FORMAT position, which performs as a write protect override switch.

When a sector is formatted, data must be first written into the sector before any valid read operation may be initiated on that sector. Thus when reformatting a normal sector into a write-protected sector, the data in the sector, if it is to be saved, must first be read into a temporary storage area while the sector is reformatted, and then rewritten into the sector after it has been reformatted.