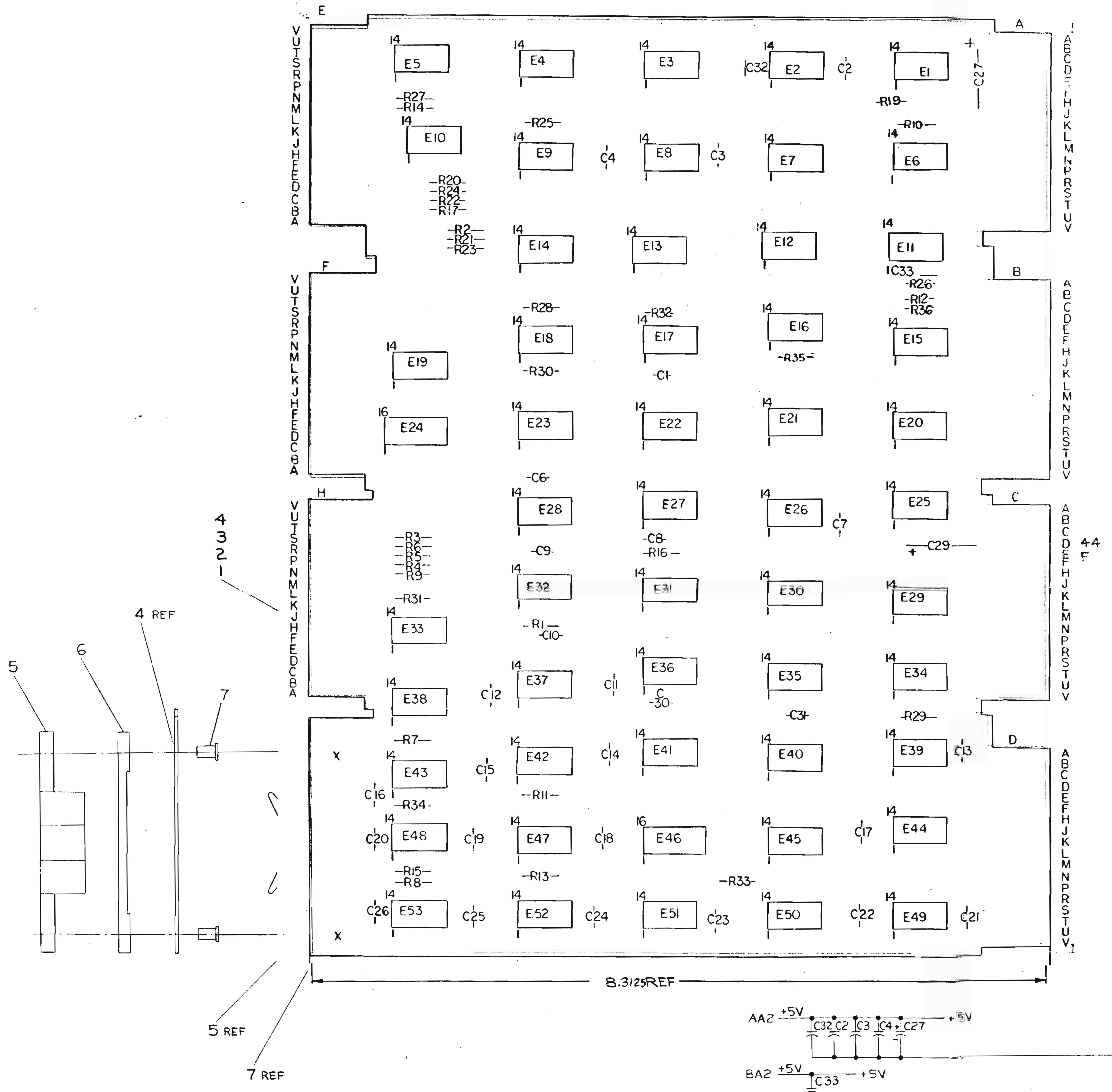
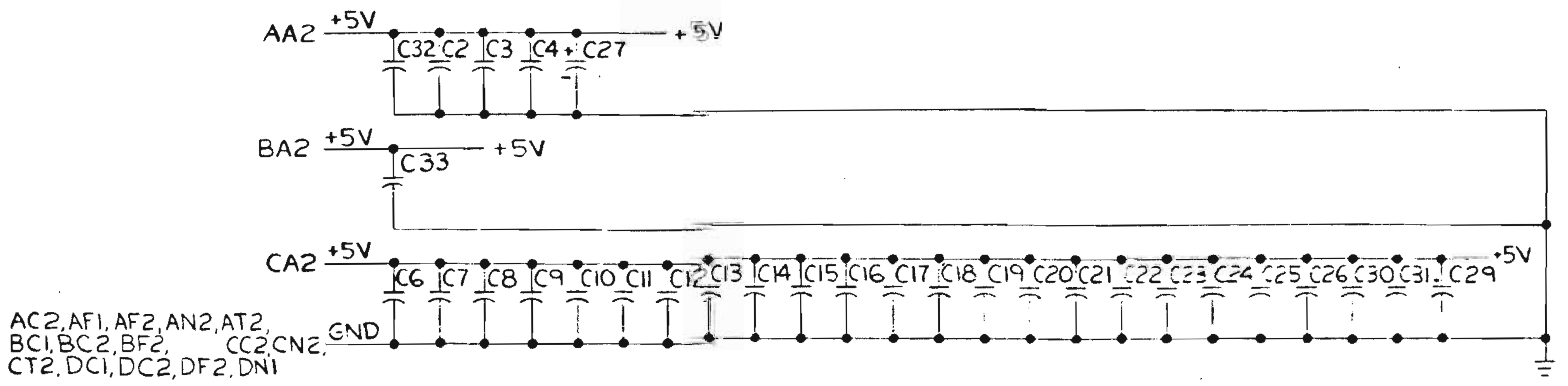
NOTES:





QTY.	REF DESIGNATION	DESCRIPTION	PART NO.
2	E40,E45	I.C. DEC 74H74	1909667
3	E18,E21,E35	I.C. DEC 74H00	1909056
2	E14,E36	I.C. DEC 74H04	1909931
1	R35	RES 100, 1/4W, 5%	[illegible]
1	E38	I.C. DEC 7486	1910011
3	E9,E11,E13	I.C. DEC 7412	1909955
1	E24	I.C. DEC 74151	1909936
4	E8,E10,E27,E28	I.C. DEC 7405	1909930
12	E1-E5,E23,E43, E44,E49,E52, E53,E15	I.C. DEC 8881	1909705
7	E6, E16,E20,E26, E34, E47,E48	I.C. DEC 7404	1909680
1	E46	I.C. DEC 8251	1909594
1	E29	I.C. DEC 384	1909486
6	E19,E22,E25,E37,E41,E51	I.C. DEC 7402	1909004
2	E7,E30	I.C. DEC 7420	1905577
2	E12,E31	I.C. DEC 7410	1905576
3	E32,E39,E42	I.C. DEC 7400	1905575
3	E17,E33,E50	I.C. DEC 7474	1905547
34	R1-R17,R19-R34,R36	RES. 470, 1/4W, 5%	1300316
29	C1-C4,C6-C26,C30-33	CAP. .01UF,100V,20% DISC	1001610
2	C27, C29	CAP. 6.8UF,35V,20% S.TANT	1000067
2		EYELETS GS4-11 STIMPSON	9006750
1		SPACER (CABLE CLAMP)	1202704
1		HANDLE, FLIP CHIP-MAGENTA	9008337-06
1		ETCHED CIRCUIT BOARD	5009278
REF		MODULE ECO HISTORY	E-MH-M8312-0-6
REF		ASSY/DRILLING HOLE LAYOUT	[illegible]
REF		X-Y COORDINATE HOLE LOC.	[illegible]

PARTS LIST

IC TYPE	GND	+5V
DEC 74151	8	16
DEC 8251	8	16
DEC 384	1	8

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTFULLY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

ITEM NO	AWG	FROM PT	TO PT

JUMPER LIST

REV	CHANGE NO	
A	M8310-00001	LOUIS KLOTZ
B	M8310 00002	LOUIS KLOTZ
C	M8310-00004	LOUIS KLOTZ
D	M8310-00005	LOUIS KLOTZ
E	M8310-00006	LOUIS KLOTZ

REVISIONS

REV COLUMN

PRINTED CIRCUIT BOARD REVISION: E

CIRCUIT SCH REVISION: D

DRN. / CHK'D. / ENG. / PROJ. ENG. / PROD. — DATE

FIRST USED ON: D-UA-KK8-E-0

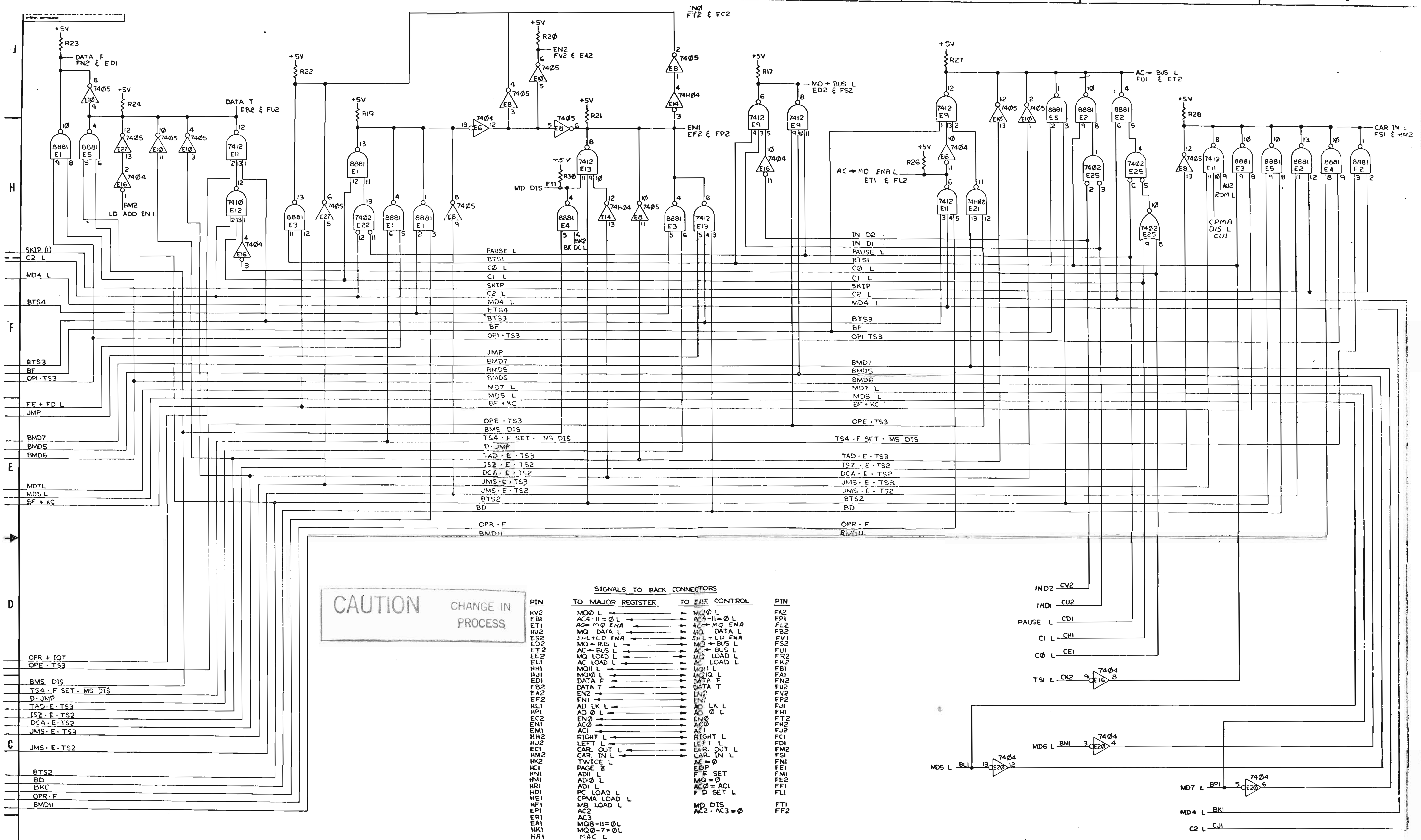
DEC NO. | EIA NO.

EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: MAJOR REG. CONT. (M8312)

SIZE | CODE | NUMBER | REV.

CAUTION
CHANGE IN PROCESS
PAGE Z
LINK L
LINK
INITIALIZE
BTP3
TAD·E L
OP1 L
LINK DATA L
LINK LOAD L
RIGHT L
LEFT L
TWICE L
ADLK L
OVFLOW L
FM2 & EC1 CAR OUT L
AD LK DIS L TO EAE
IOT L
MD7 L
MD5 L
BMD8
BMD9
BMD10
F SET L
PC LOAD L
BUS STROBE
MD4 L
CPMA DIS L
MAC L
PWR OK
FR2 & EE2 MQ LOAD L
CPMA LOAD L
MB LOAD L
DR2 PULSE LA
AC LOAD L
SKIP L
C2 L
OV H
INIT
BTS4
BTP2
TAD·E L
BTS3
BF
OF1·TS3
FE+FD L
JMP
TP1
JMS·E
BMD7
KC L
OPE
TP4·MALC
BTS3
OV H
BTP2
F SET L
TAD·E L
AND·E L
DCA·E L
ISZ·E·TS3
OPR+IOT L
C/F·R·F L
AC=0
OPI L
OP2·TS3
BF+KC
AND·E·TS3
MD8L
SKIP
MD4
BMD5
BMD6
MD7 L
MD5 L
BF+KC
OPR+IOT
OPE·TS3
BMS DIS
TS4·F SET·MS DIS
D·JMP
TAD·E·TS3
ISZ·E·TS2
DCA·E·TS2
JMS·E·TS3
JMS·E·TS2
BTS2
BD
BKC
OPR·F
BMD11
FIRST USED ON OPTION MODEL PDP 8/E
EQUIPMENT CORPORATION
M830 MAJOR REG. CONT.
A-ML-KK8-E
E CS M830-0-1
REV. E



SIGNALS TO BACK CONNECTORS

PIN	TO MAJOR REGISTER	TO EAE CONTROL	PIN
HV2	MQØ L	MQØ L	FA2
EB1	AC4-11 = Ø L	AC4-11 = Ø L	FP1
ET1	AC → MQ ENA	AC → MQ ENA	FL2
HU2	MQ DATA L	MQ DATA L	FB2
ES2	SHL + LD ENA	SHL + LD ENA	FV1
ED2	MQ → BUS L	MQ → BUS L	FS2
ET2	AC → BUS L	AC → BUS L	FU1
EE2	MQ LOAD L	MQ LOAD L	FR2
EL1	AC LOAD L	AC LOAD L	FK2
HH1	MQ11 L	MQ11 L	FB1
HJ1	MQ1Ø L	MQ1Ø L	FA1
ED1	DATA F	DATA F	FN2
EB2	DATA T	DATA T	FU2
EA2	EN2	EN2	FV2
EF2	EN1	EN1	FP2
HL1	AD LK L	AD LK L	FJ1
HP1	AD Ø L	AD Ø L	FH1
EC2	ENØ	ENØ	FT2
EN1	ACØ	ACØ	FH2
EM1	AC1	AC1	FJ2
HH2	RIGHT L	RIGHT L	FC1
HJ2	LEFT L	LEFT L	FD1
EC1	CAR. OUT L	CAR. OUT L	FM2
HM2	CAR. IN L	CAR. IN L	FS1
HK2	TWICE L	AC = Ø	FN1
HC1	PAGE Z	EOP	FE1
HN1	AD11 L	F E SET	FM1
HM1	AD1Ø L	MQ = Ø	FE2
HR1	AD1 L	ACØ = AC1	FF1
HD1	PC LOAD L	F D SET L	FL1
HE1	CPMA LOAD L		
HF1	MB LOAD L	MD DIS	FT1
EP1	AC2	AC2 · AC3 = Ø	FF2
ER1	AC3		
EA1	MQ8-11 = Ø L		
HK1	MQØ-7 = Ø L		
HA1	MAC L		

RIGHT L	LEFT L	TWICE L	PAGE Z	DATA TO REGISTER	USE
L	L	L	L	MA ← Ø-4 MO ← 5-11	PAGE ADDRESSING
L	L	H	X	MBX ∧ ACX	AND
L	H	L	X	ADDER (X-2)	RTR
L	H	H	X	ADDER (X-1)	RAR
H	L	L	X	ADDER (X+2)	RTL
H	L	H	X	ADDER (X+1)	RAL
H	H	L	X	ADDER (X+6)	BYTE SWAP
H	H	H	X	ADDER X	NO SHIFT
L	L	L	H	Ø ← MAØ-4 MD ← MA5-11	PG Ø ADDRESSING

ENØ	EN1	EN2	INPUT TO ADDER
L	L	L	PC
L	L	H	MD
L	H	L	MQ
L	H	H	MA
H	X	X	H (ARITHMETIC ZERO)

DATA T	DATA F	INPUT TO ADDER
[illegible]	L	DATA BUS NOT
[illegible]	H	DATA BUS
H	L	H (ARITHMETIC ZERO)
H	H	L (ARITHMETIC ONE)

BIT X OF THE REGISTER SELECTED HERE IS ADDED TO BIT X OF THE DATA BUS AS SELECTED HERE AND THE SUM (ADDER X) IS FED TO A MULTIPLEXER TO BE DECODED AS ABOVE. THE OUTPUT OF THIS MULTIPLEXER IS LOADED INTO WHICH EVER REGISTER IS CLOCKED.

SHL ENA L	AC → MQ ENA L	DATA → MQ
L	L	MQX+1 Ø-1Ø MQ DATA → MQ11
L	H	MQX+1 Ø-1Ø MQ DATA → MQ11
H	L	AC (IN COMPLEMENT TO REDEFINE)
H	H	I (Ø → MQ)

FIRST USED ON OPTION MODEL: PDP 8/E

QTY.	DESCRIPTION	PART NO.
	PARTS LIST	

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL

DRN / CHK'D / ENG / PROJ. ENG. / PROD. / DATE

NEXT HIGHER ASSY: A-ML-KK8-E

EQUIPMENT CORPORATION, MAYNARD MASSACHUSETTS

TITLE: M8310 MAJOR REG. CONT.

FIRST USED ON OPTION MODEL PDP 8/E

QTY	DESCRIPTION	PART NO.	ITEM NO.
	PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES

MATERIAL

EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE M830 MAJOR REG CONT.